FIG. 1

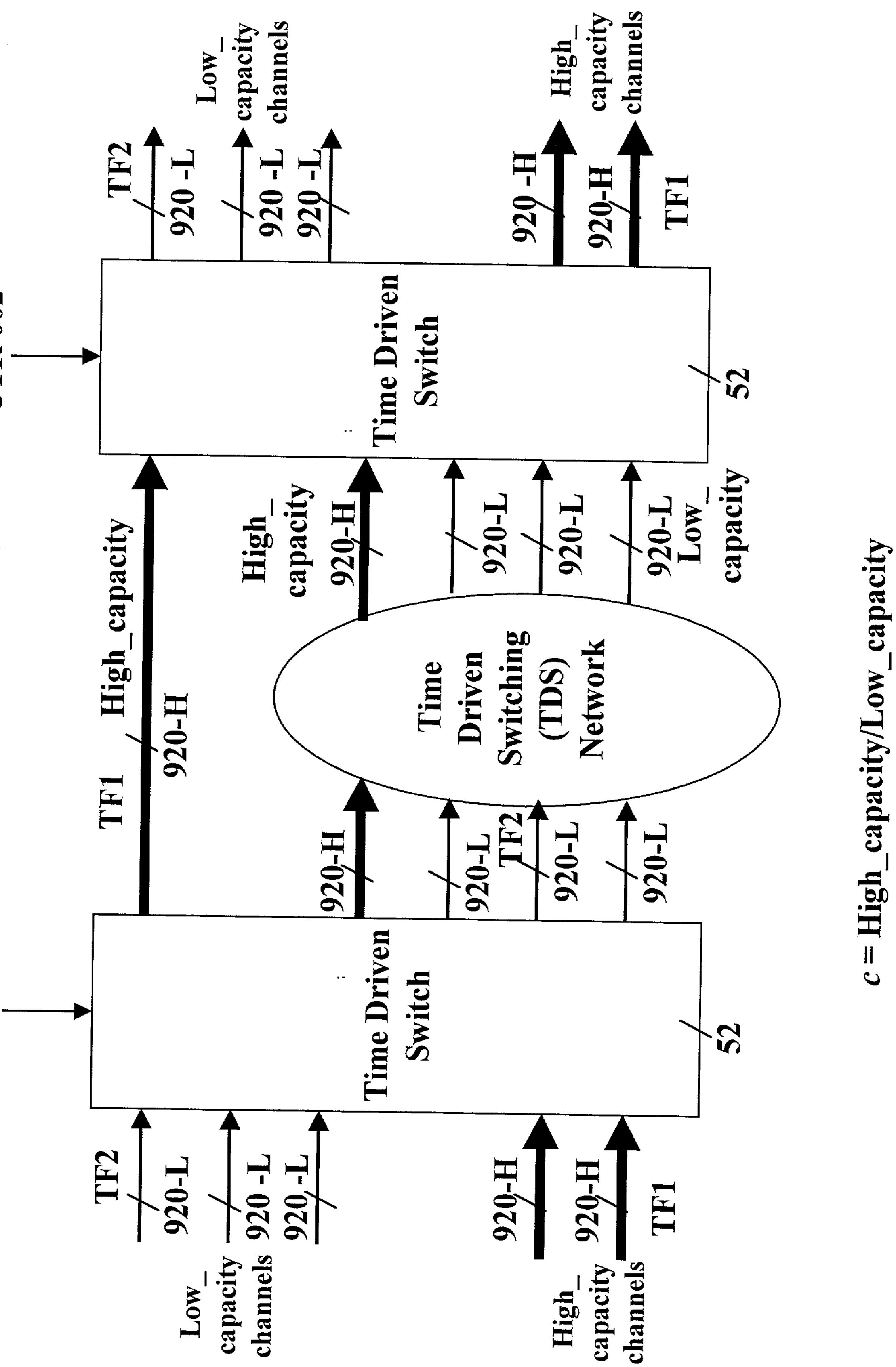

CTR 002
Time Driven Switch
52
CTR 002
Time Driven Switch
52
Time Driven Switching (TDS) Network
TF1
TF2
920-H
920-L
High_capacity
Low_capacity
High_ capacity channels
Low_ capacity channels
c = High_capacity/Low_capacity

FIG. 2

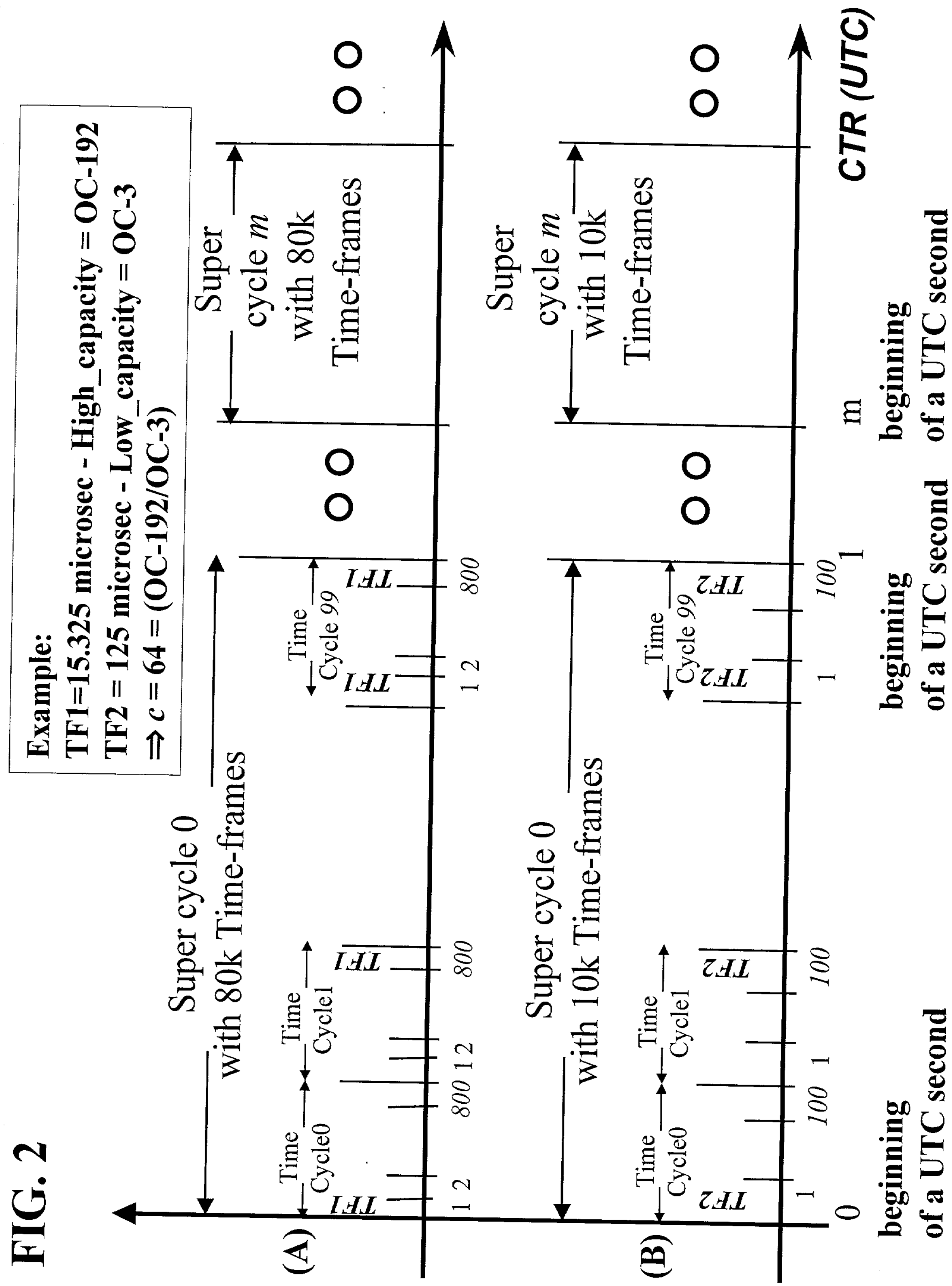
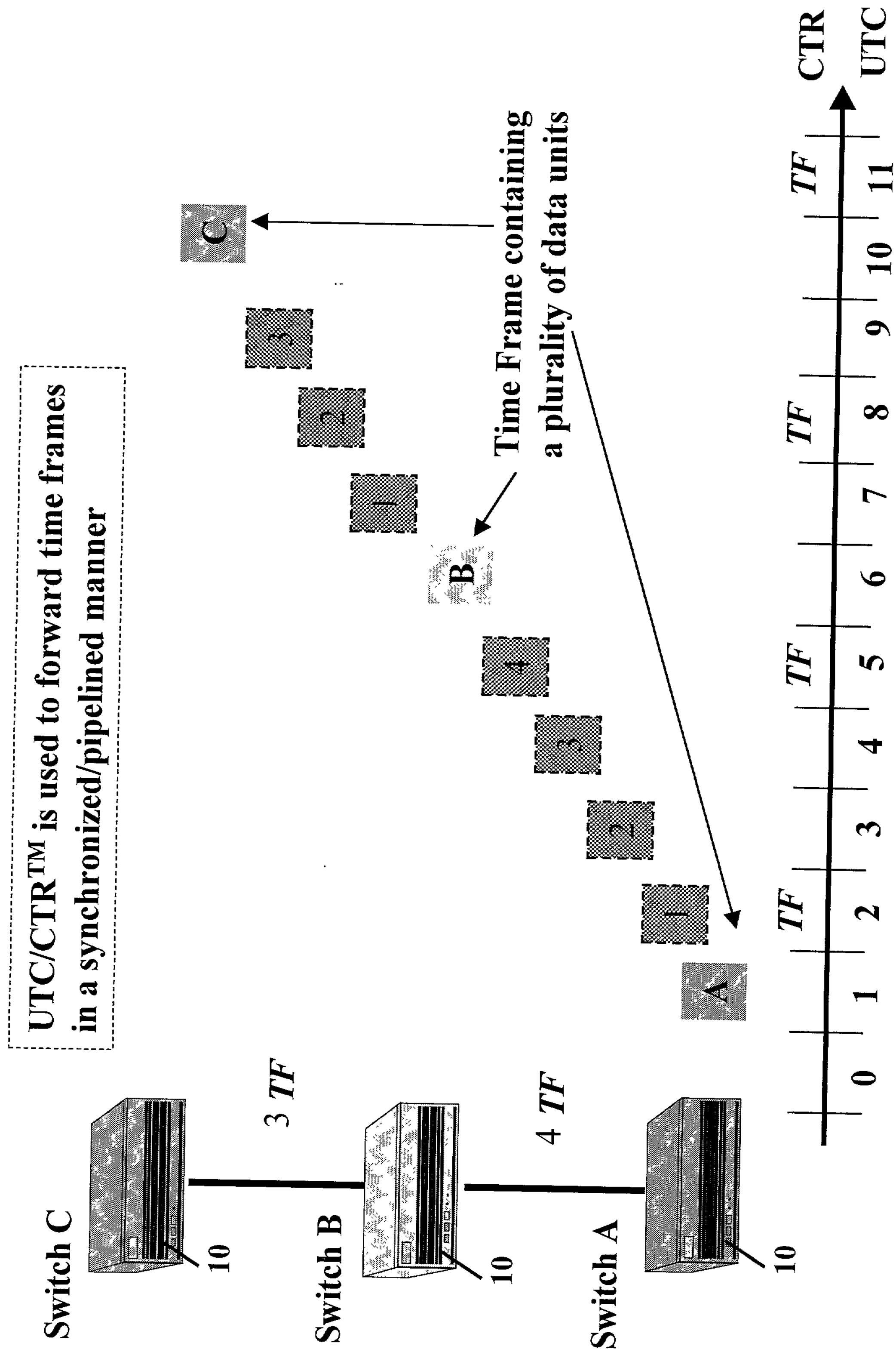

Example:
TF1=15.325 microsec - High_capacity = OC-192
TF2 = 125 microsec - Low_capacity = OC-3
⇒ c = 64 = (OC-192/OC-3)
(A)
Super cycle 0 with 80k Time-frames
Time Cycle0
Time Cycle1
Time Cycle 99
TF1
1 2
800
800 1 2
Super cycle m with 80k Time-frames
(B)
Super cycle 0 with 10k Time-frames
Super cycle m with 10k Time-frames
TF2
1
100
100 1
0
1
m
beginning of a UTC second
CTR (UTC)

FIG. 3


Switch C
Switch B
Switch A
10
3 TF
4 TF
UTC/CTR™ is used to forward time frames in a synchronized/pipelined manner
Time Frame containing a plurality of data units
A
1
2
3
4
B
1
2
3
C
TF
0
1
2
3
4
5
6
7
8
9
10
11
CTR
UTC

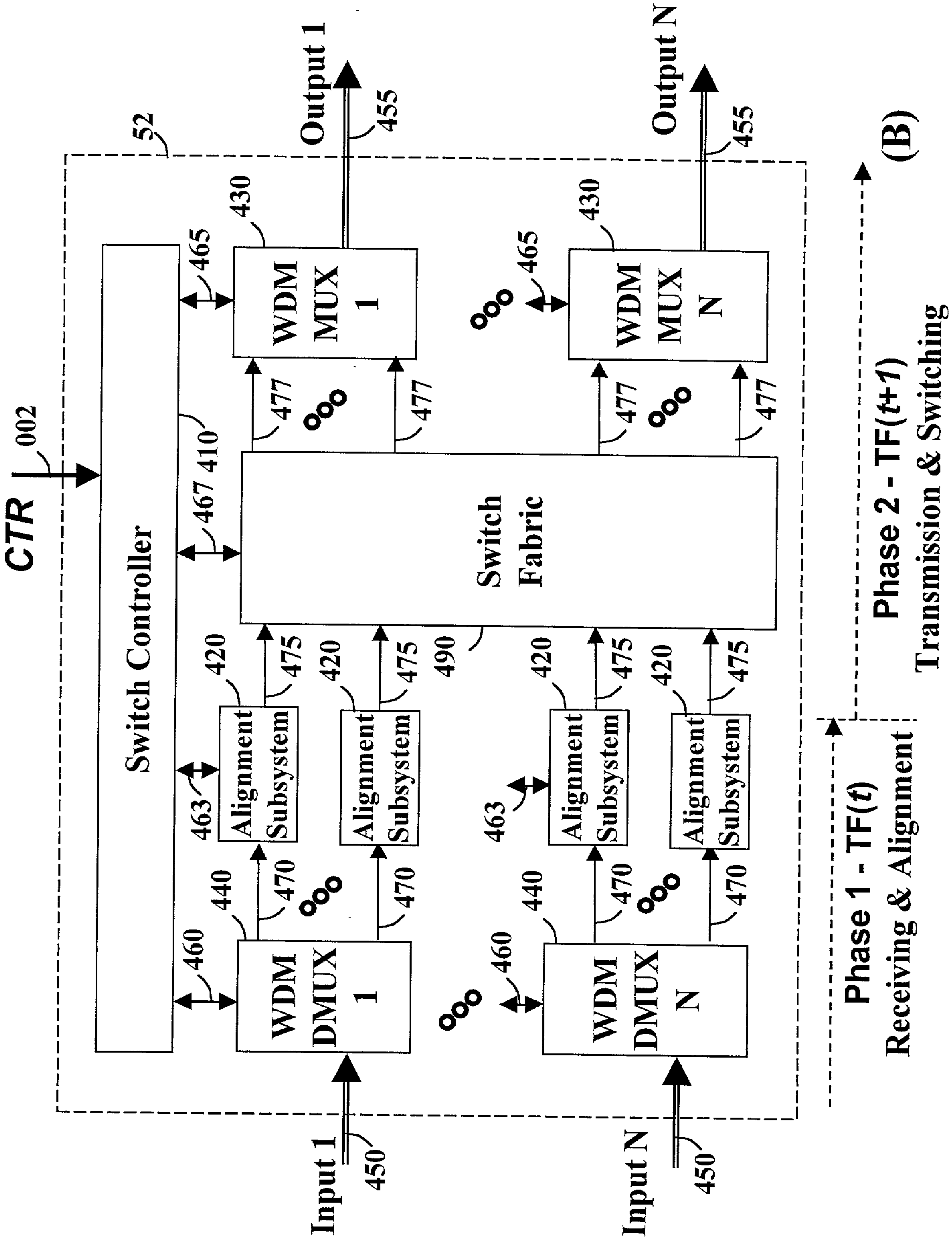

CTR
002
52
Switch Controller
Switch Fabric
WDM DMUX 1
WDM DMUX N
Alignment Subsystem
WDM MUX 1
WDM MUX N
Input 1
Input N
Output 1
Output N
450
455
460
463
465
467
410
420
430
440
470
475
477
490
Phase 1 - TF(t)
Receiving & Alignment
Phase 2 - TF(t+1)
Transmission & Switching
(B)

FIG. 4

FIG. 5

Two time intervals: SC1_length·TF1 = 1 UTC second

- SC2_length·TF2 = 1 UTC second
- TF2 = (SC1_length / SC2_length) · TF1 = k · TF1, where the time cycles of TF1 and TF2 are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

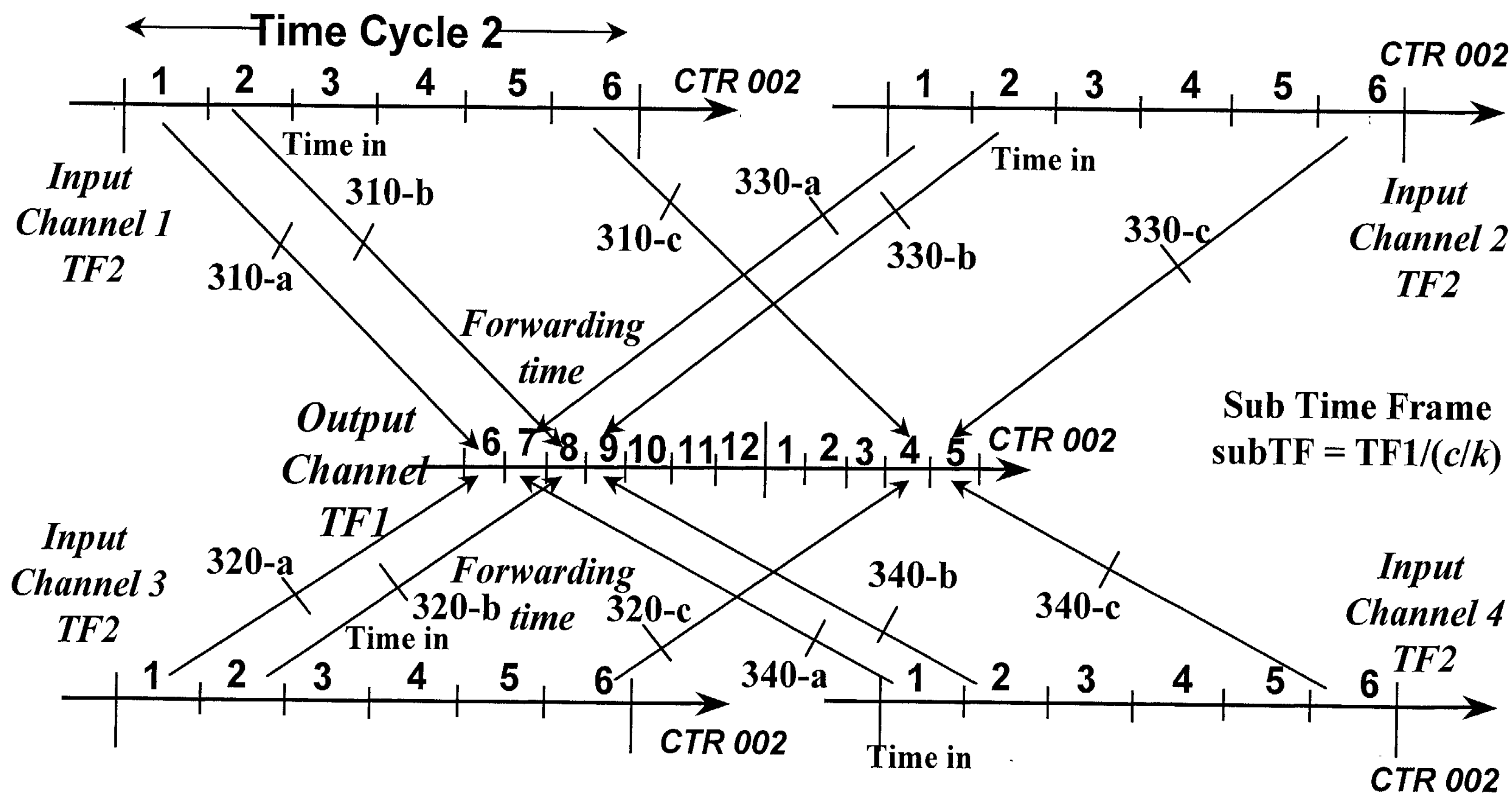


FIG. 6

Two time intervals: $SC1\_length \cdot TF1 = 1$ UTC second

- $SC2\_length \cdot TF2 = 1$ UTC second
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the time cycles of $TF1$ and $TF2$ are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

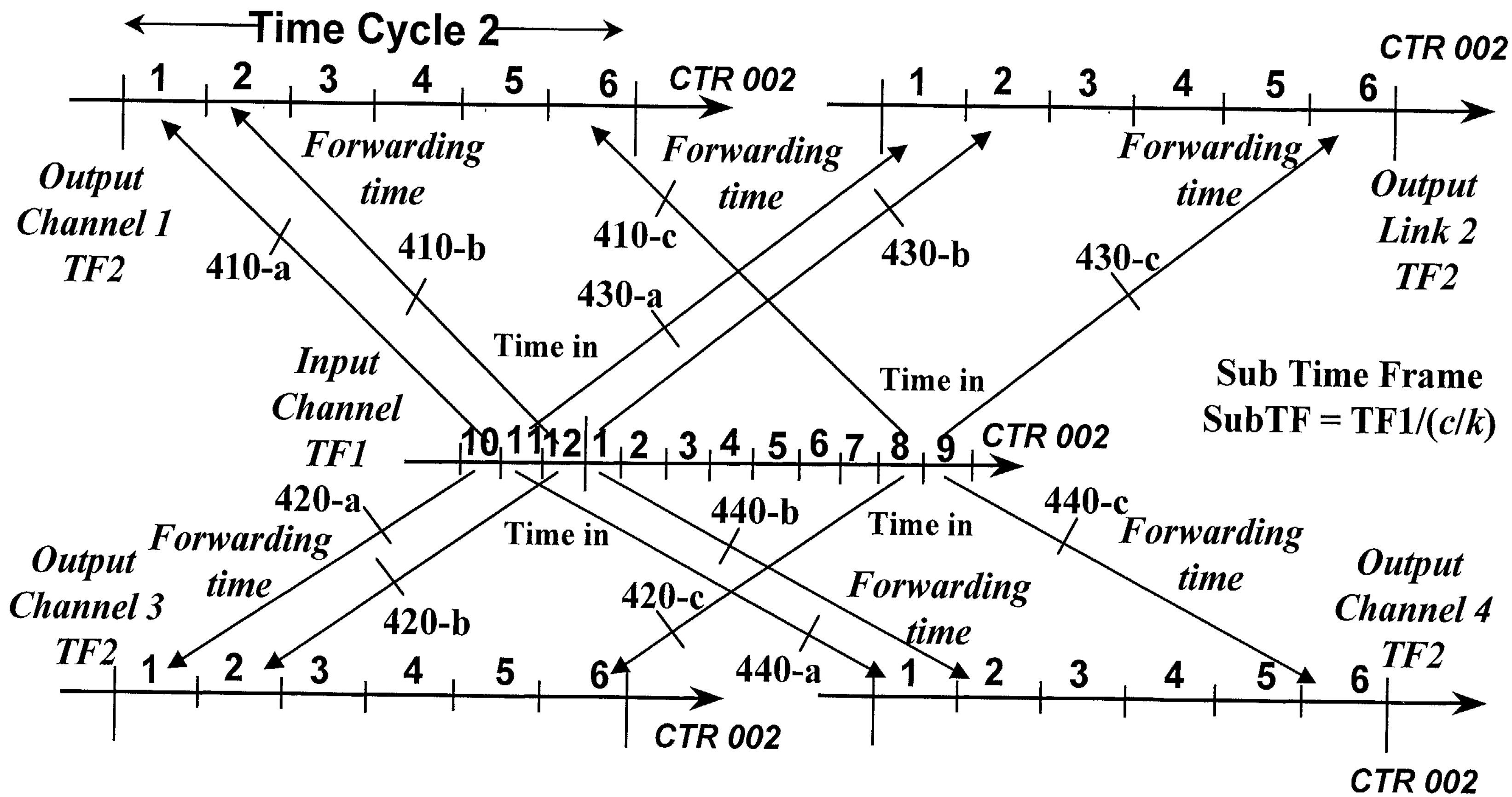


FIG. 7

Two time intervals: $SC1\_length \cdot TF1 = 1$ UTC second

- $SC2\_length \cdot TF2 = 1$ UTC second
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the time cycles of $TF1$ and $TF2$ are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

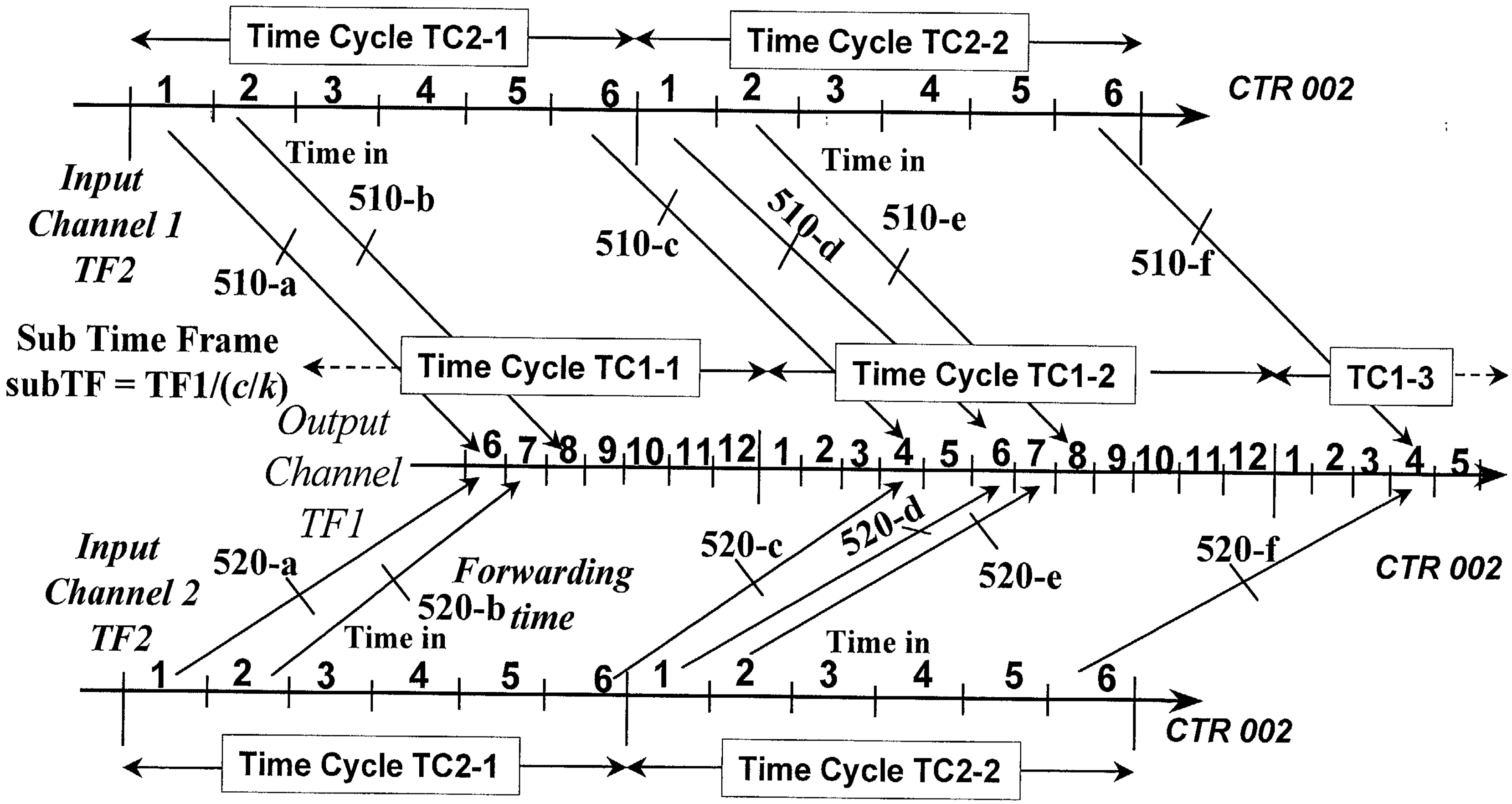
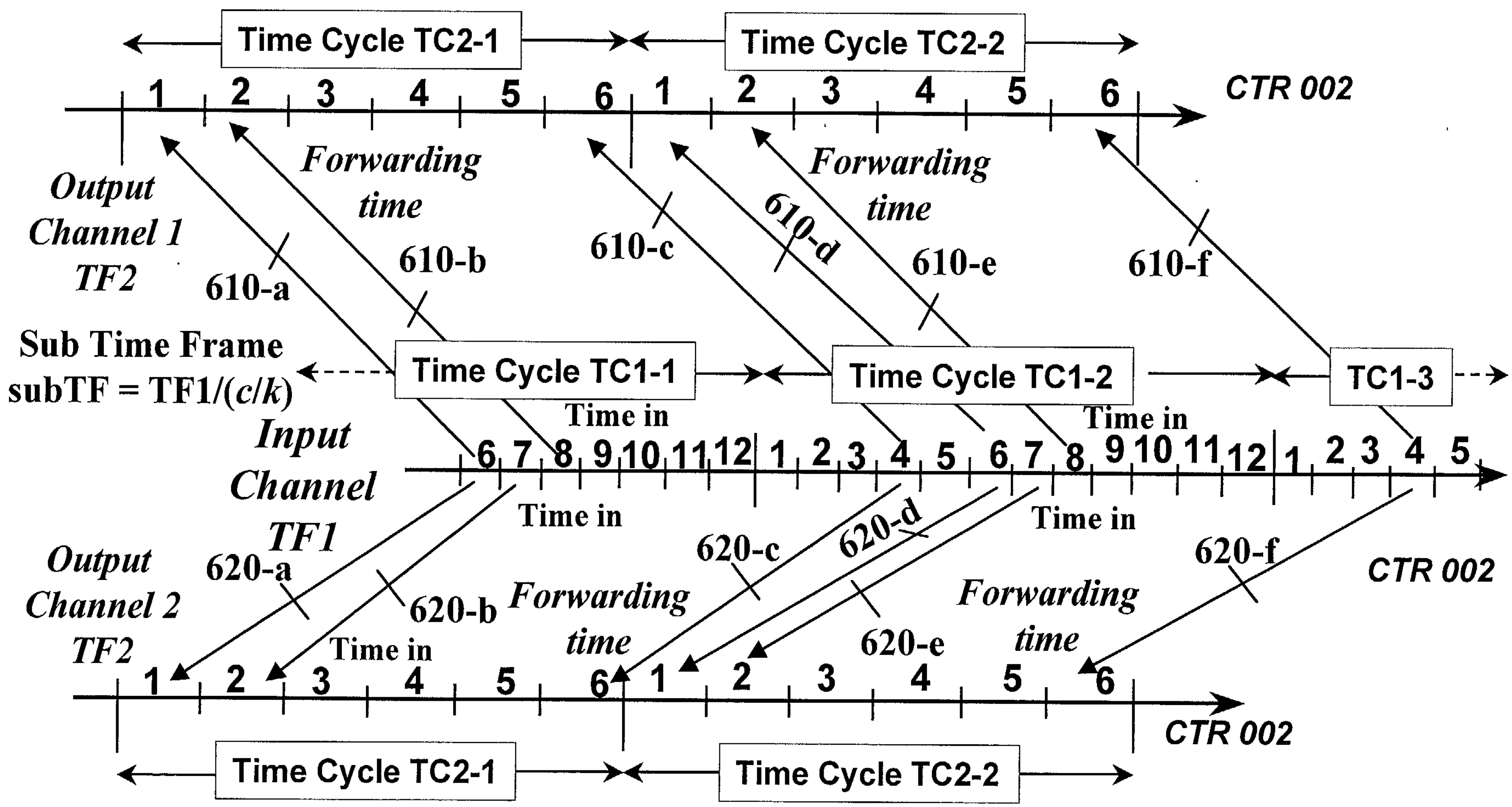


FIG. 8

Two time intervals: $SC1\_length \cdot TF1 = 1$ UTC second

- $SC2\_length \cdot TF2 = 1$ UTC second
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the time cycles of $TF1$ and $TF2$ are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):



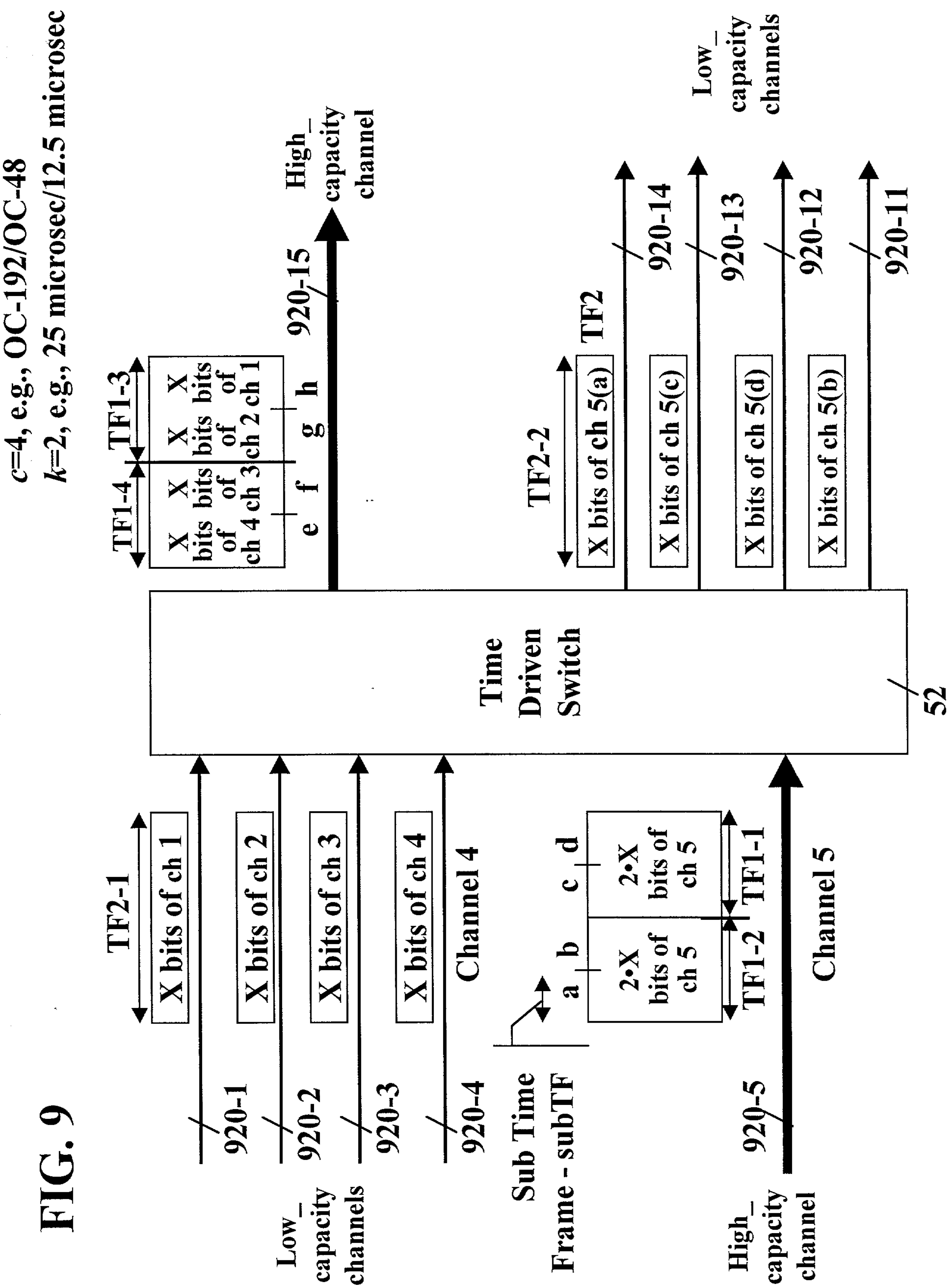
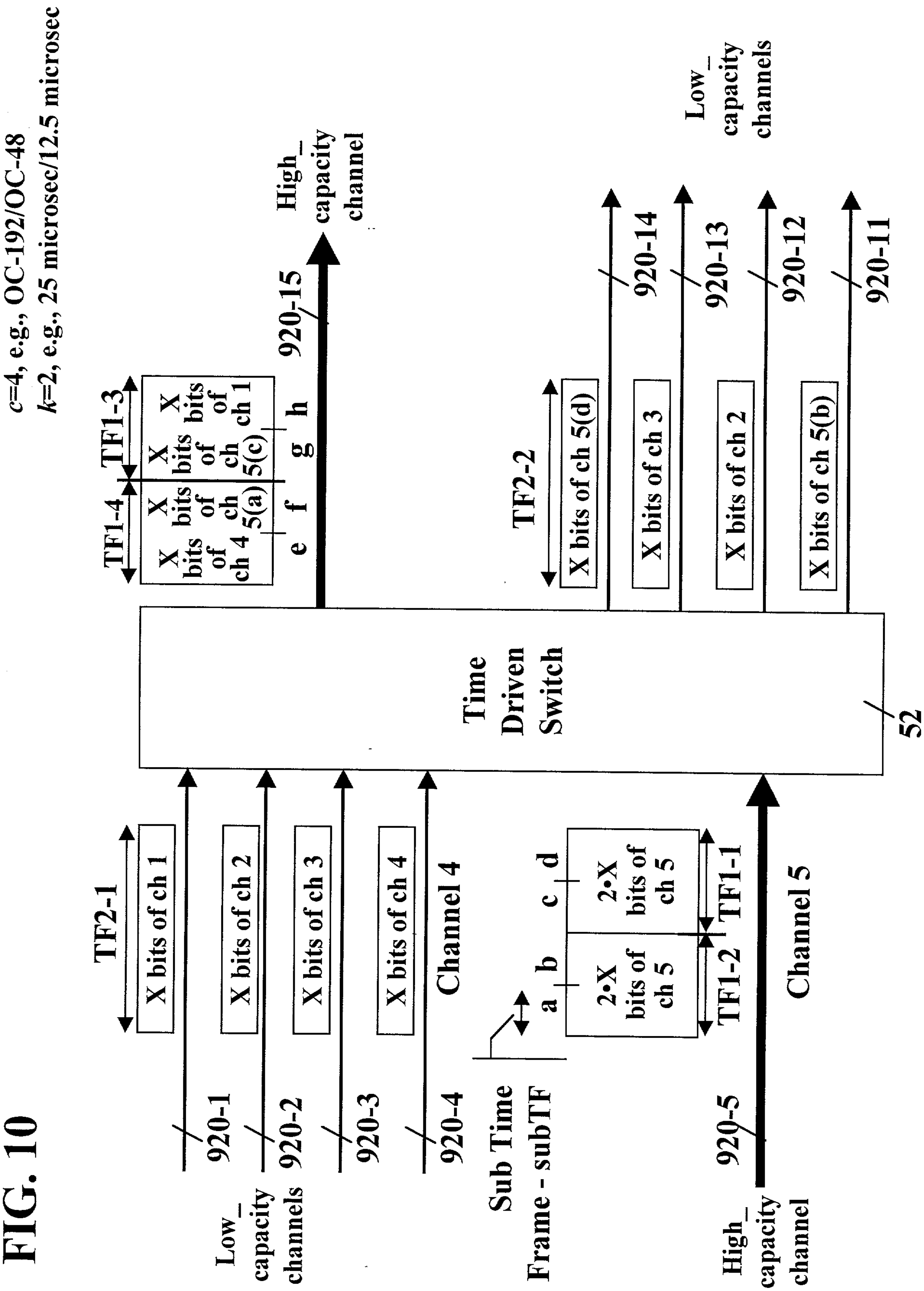

c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec
TF2-1
X bits of ch 1
X bits of ch 2
X bits of ch 3
X bits of ch 4
Channel 4
920-1
920-2
920-3
920-4
Low_ capacity channels
Sub Time Frame - subTF
a
b
c
d
2•X bits of ch 5
2•X bits of ch 5
TF1-2
TF1-1
Channel 5
920-5
High_ capacity channel
Time Driven Switch
52
TF1-4
TF1-3
X bits of ch 4
X bits of ch 3
X bits of ch 2
X bits of ch 1
e
f
g
h
920-15
High_ capacity channel
TF2-2
TF2
X bits of ch 5(a)
X bits of ch 5(c)
X bits of ch 5(d)
X bits of ch 5(b)
920-14
920-13
920-12
920-11
Low_ capacity channels

FIG. 9

FIG. 10


c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec
Time Driven Switch
52
Low_ capacity channels
920-1
920-2
920-3
920-4
TF2-1
X bits of ch 1
X bits of ch 2
X bits of ch 3
X bits of ch 4
Channel 4
Sub Time Frame - subTF
a
b
c
d
2•X bits of ch 5
2•X bits of ch 5
TF1-2
TF1-1
Channel 5
High_ capacity channel
920-5
TF1-4
TF1-3
X bits of ch 4
X bits of ch 5(a)
X bits of ch 5(c)
X bits of ch 1
e
f
g
h
920-15
High_ capacity channel
TF2-2
X bits of ch 5(d)
X bits of ch 3
X bits of ch 2
X bits of ch 5(b)
920-14
920-13
920-12
920-11
Low_ capacity channels

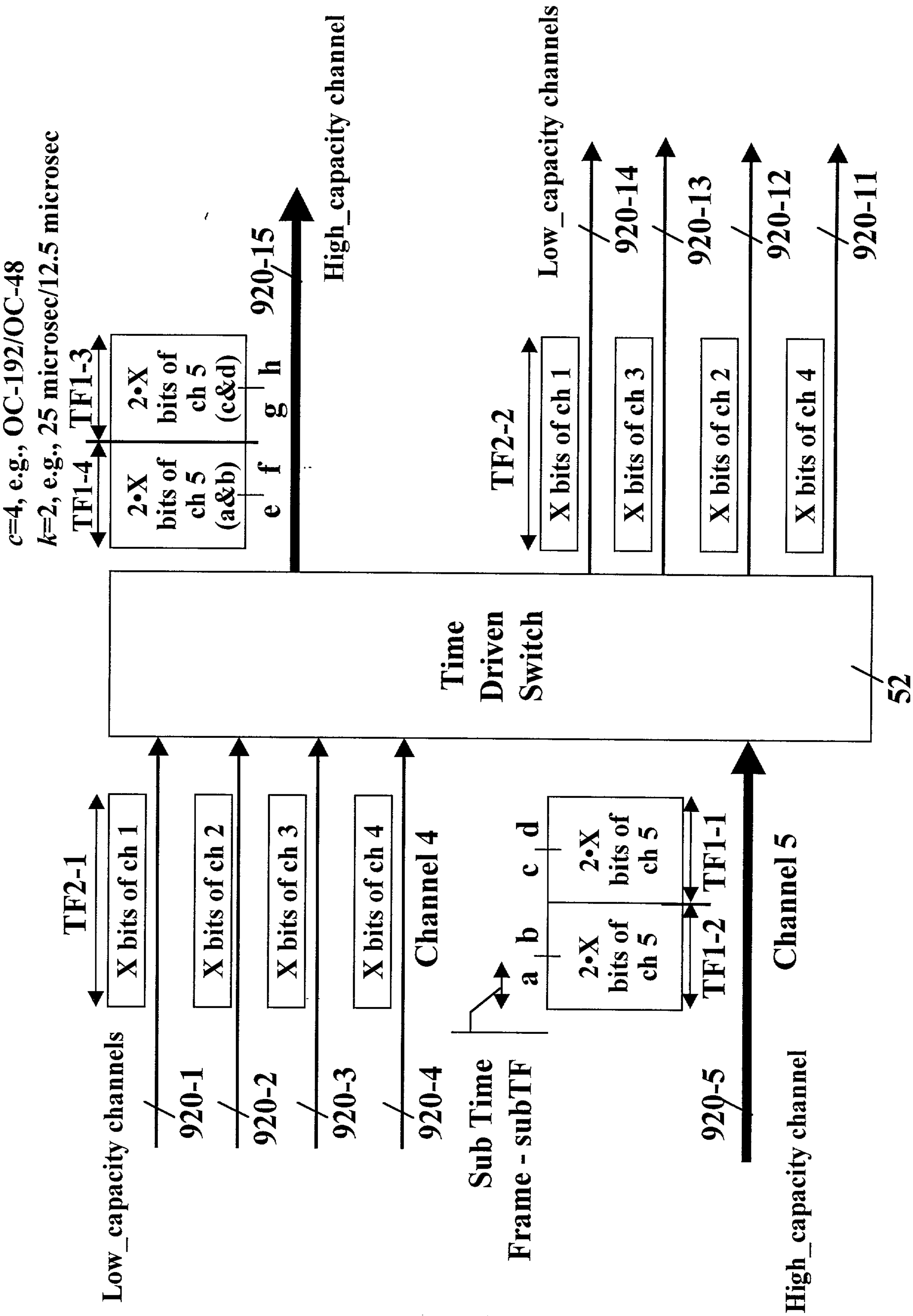

c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec
Low_capacity channels
920-1
920-2
920-3
920-4
TF2-1
X bits of ch 1
X bits of ch 2
X bits of ch 3
X bits of ch 4
Channel 4
Sub Time Frame - subTF
a b c d
2•X bits of ch 5
2•X bits of ch 5
TF1-2
TF1-1
920-5
Channel 5
High_capacity channel
Time Driven Switch
52
TF1-4
TF1-3
2•X bits of ch 5 (a&b)
2•X bits of ch 5 (c&d)
e f g h
920-15
High_capacity channel
TF2-2
X bits of ch 1
X bits of ch 3
X bits of ch 2
X bits of ch 4
Low_capacity channels
920-14
920-13
920-12
920-11

FIG. 11

FIG. 12

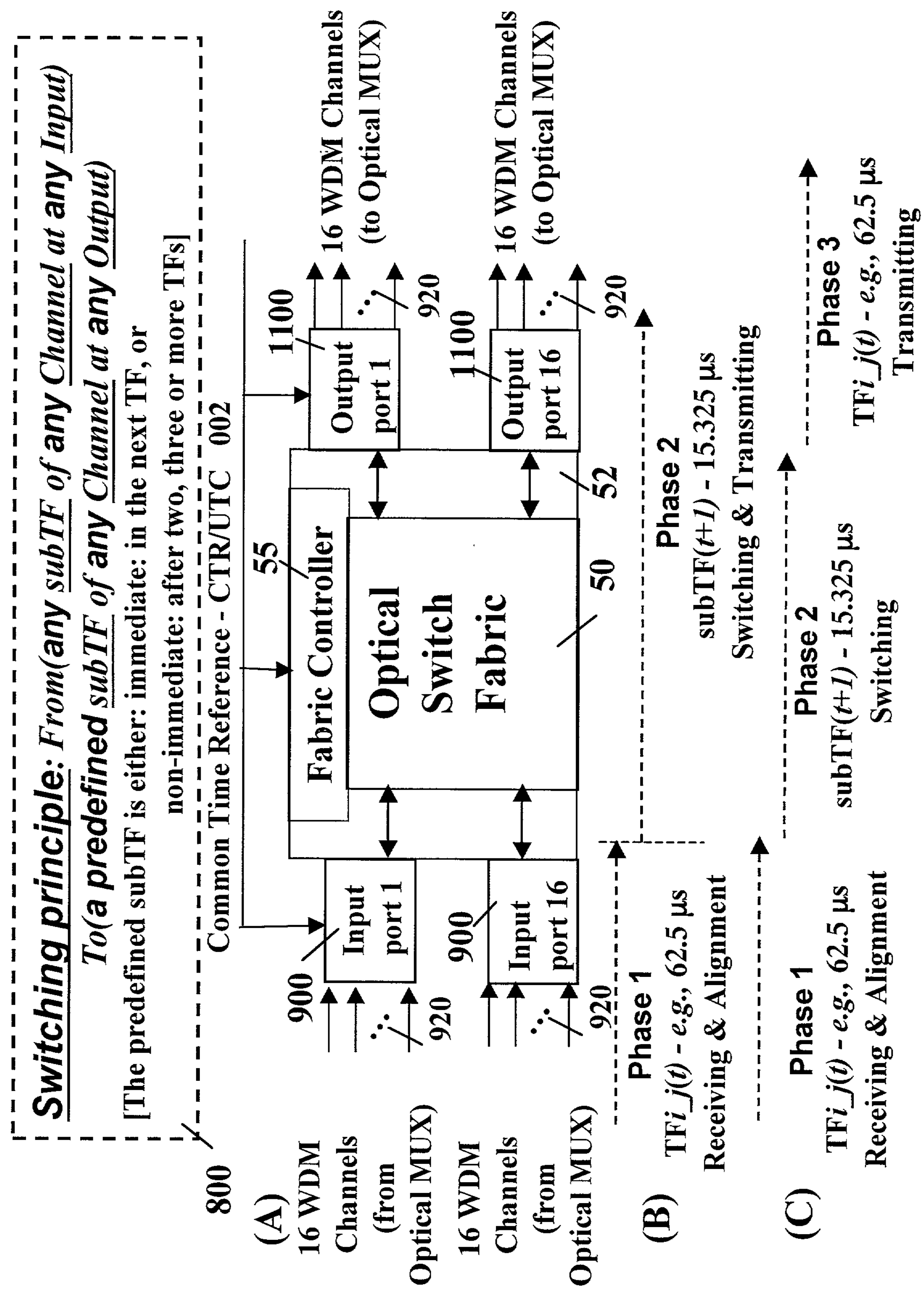

Switching principle: From(any subTF of any Channel at any Input)
To(a predefined subTF of any Channel at any Output)
[The predefined subTF is either: immediate: in the next TF, or
non-immediate: after two, three or more TFs]
800
Common Time Reference - CTR/UTC 002
(A)
16 WDM Channels (from Optical MUX)
900
Input port 1
920
16 WDM Channels (from Optical MUX)
900
Input port 16
920
55
Fabric Controller
Optical Switch Fabric
50
52
1100
Output port 1
920
16 WDM Channels (to Optical MUX)
1100
Output port 16
920
16 WDM Channels (to Optical MUX)
(B)
Phase 1
TFi_j(t) - e.g., 62.5 µs
Receiving & Alignment
Phase 2
subTF(t+1) - 15.325 µs
Switching & Transmitting
(C)
Phase 1
TFi_j(t) - e.g., 62.5 µs
Receiving & Alignment
Phase 2
subTF(t+1) - 15.325 µs
Switching
Phase 3
TFi_j(t) - e.g., 62.5 µs
Transmitting

FIG. 13

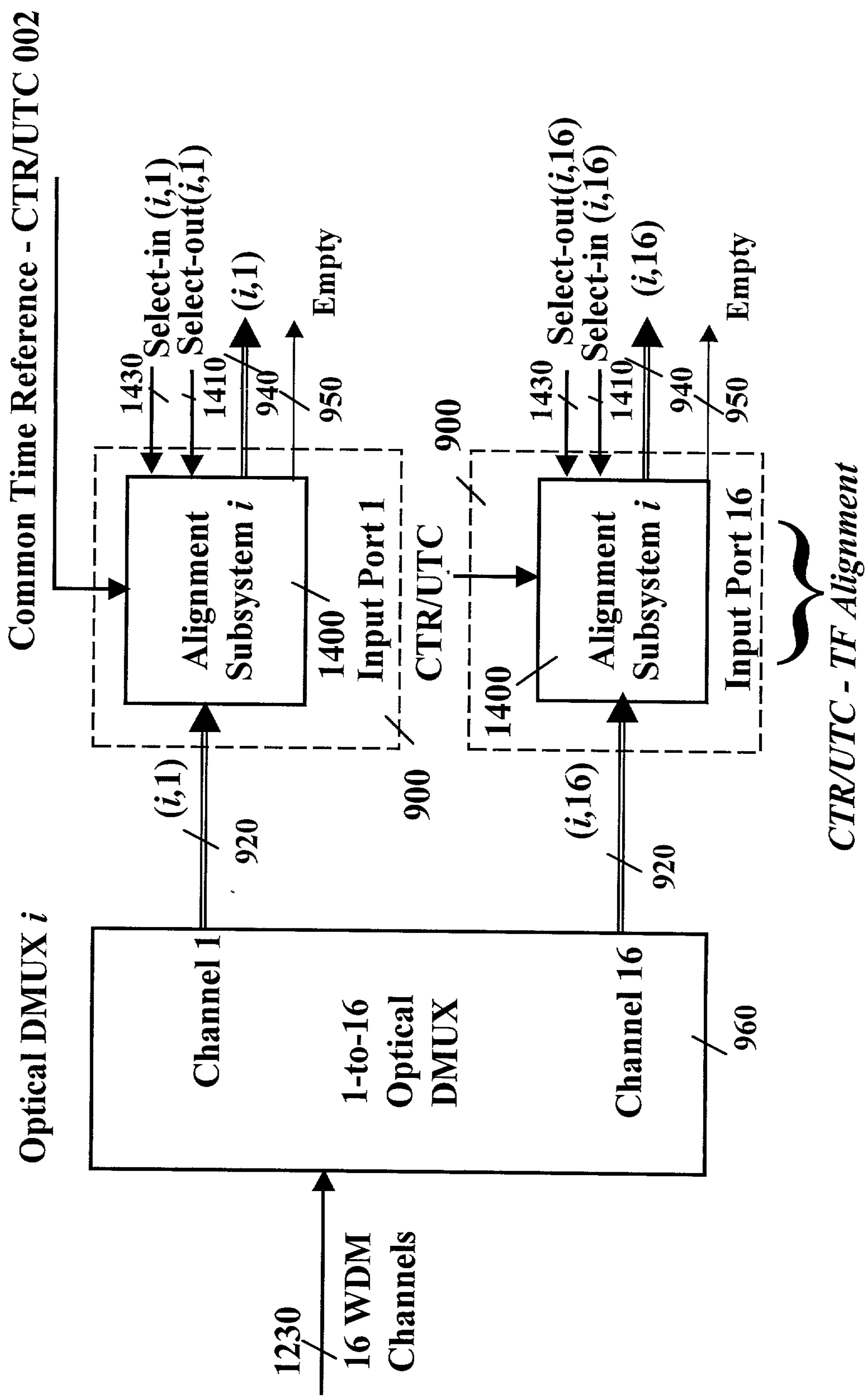
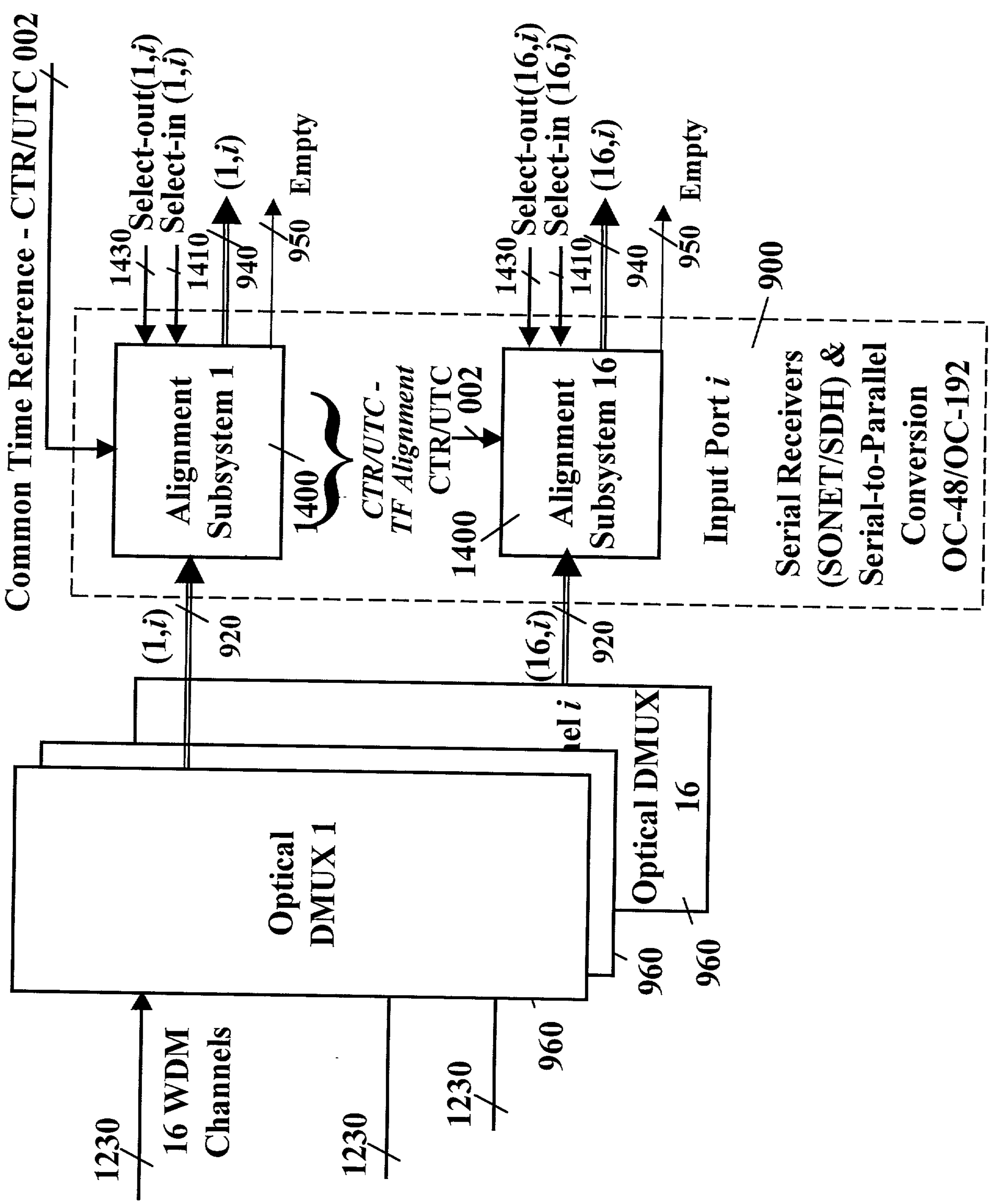

Common Time Reference - CTR/UTC 002
Optical DMUX *i*
1-to-16 Optical DMUX
Channel 1
Channel 16
960
1230
16 WDM Channels
(*i*,1)
920
(*i*,16)
920
900
900
Alignment Subsystem *i*
1400
Input Port 1
Input Port 16
CTR/UTC
1430
1410
940
950
Select-in (*i*,1)
Select-out(*i*,1)
(*i*,1)
Empty
Select-out(*i*,16)
Select-in (*i*,16)
(*i*,16)
Empty
CTR/UTC - TF Alignment

FIG. 14


Common Time Reference - CTR/UTC 002
Select-out(1,i)
Select-in (1,i)
(1,i)
Empty
1430
1410
940
950
Alignment Subsystem 1
1400
CTR/UTC - TF Alignment
CTR/UTC 002
Select-out(16,i)
Select-in (16,i)
(16,i)
Empty
Alignment Subsystem 16
Input Port i
Serial Receivers (SONET/SDH) & Serial-to-Parallel Conversion OC-48/OC-192
900
920
(1,i)
(16,i)
Optical DMUX 1
Optical DMUX 16
960
1230
16 WDM Channels

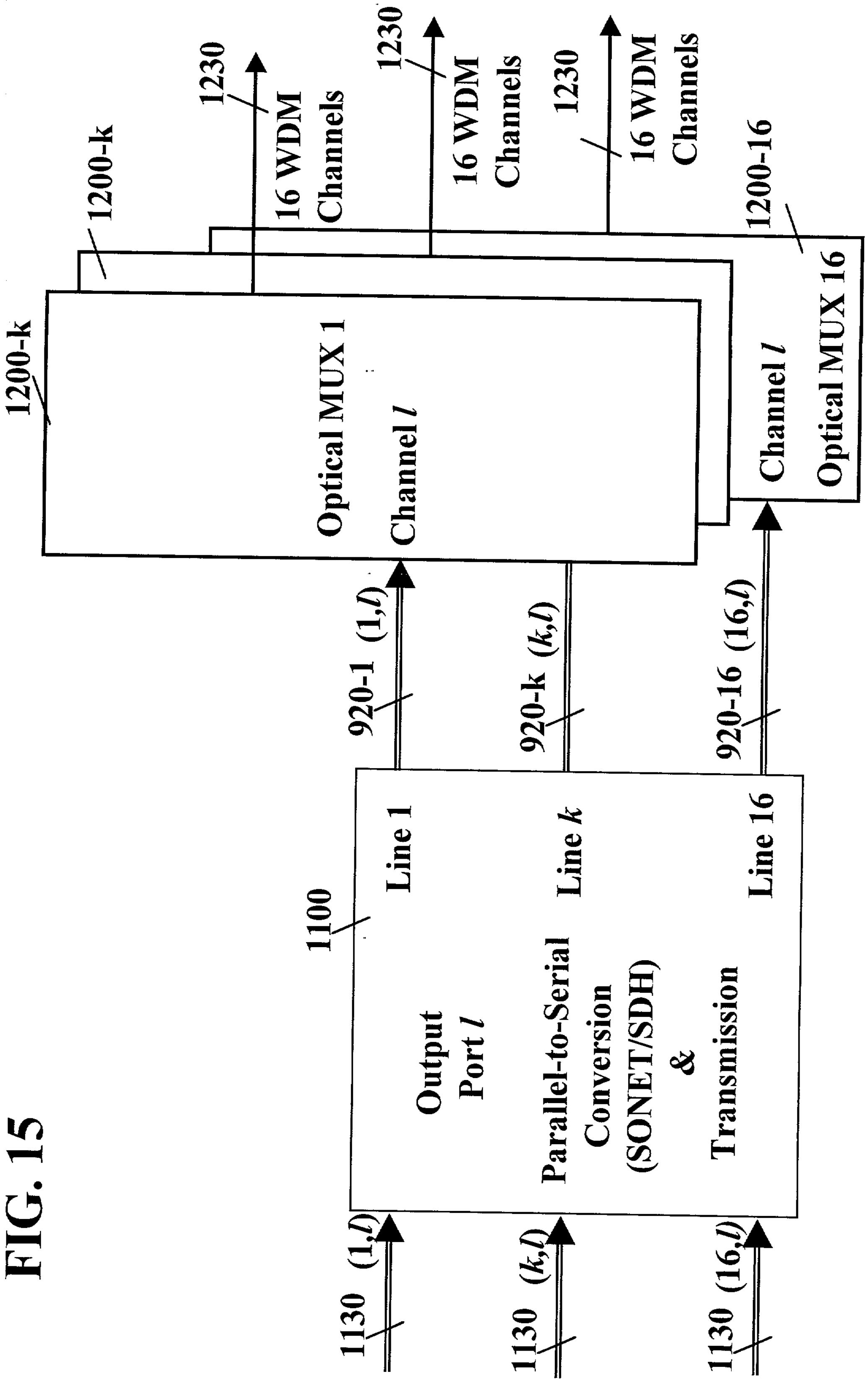

1200-k
1200-k
1230
16 WDM Channels
1230
16 WDM Channels
1230
16 WDM Channels
1200-16
Optical MUX 1
Channel *l*
Channel *l*
Optical MUX 16
920-1 (1,*l*)
920-k (*k*,*l*)
920-16 (16,*l*)
1100
Line 1
Line *k*
Line 16
Output Port *l*
Parallel-to-Serial Conversion (SONET/SDH) & Transmission
1130 (1,*l*)
1130 (*k*,*l*)
1130 (16,*l*)

FIG. 15

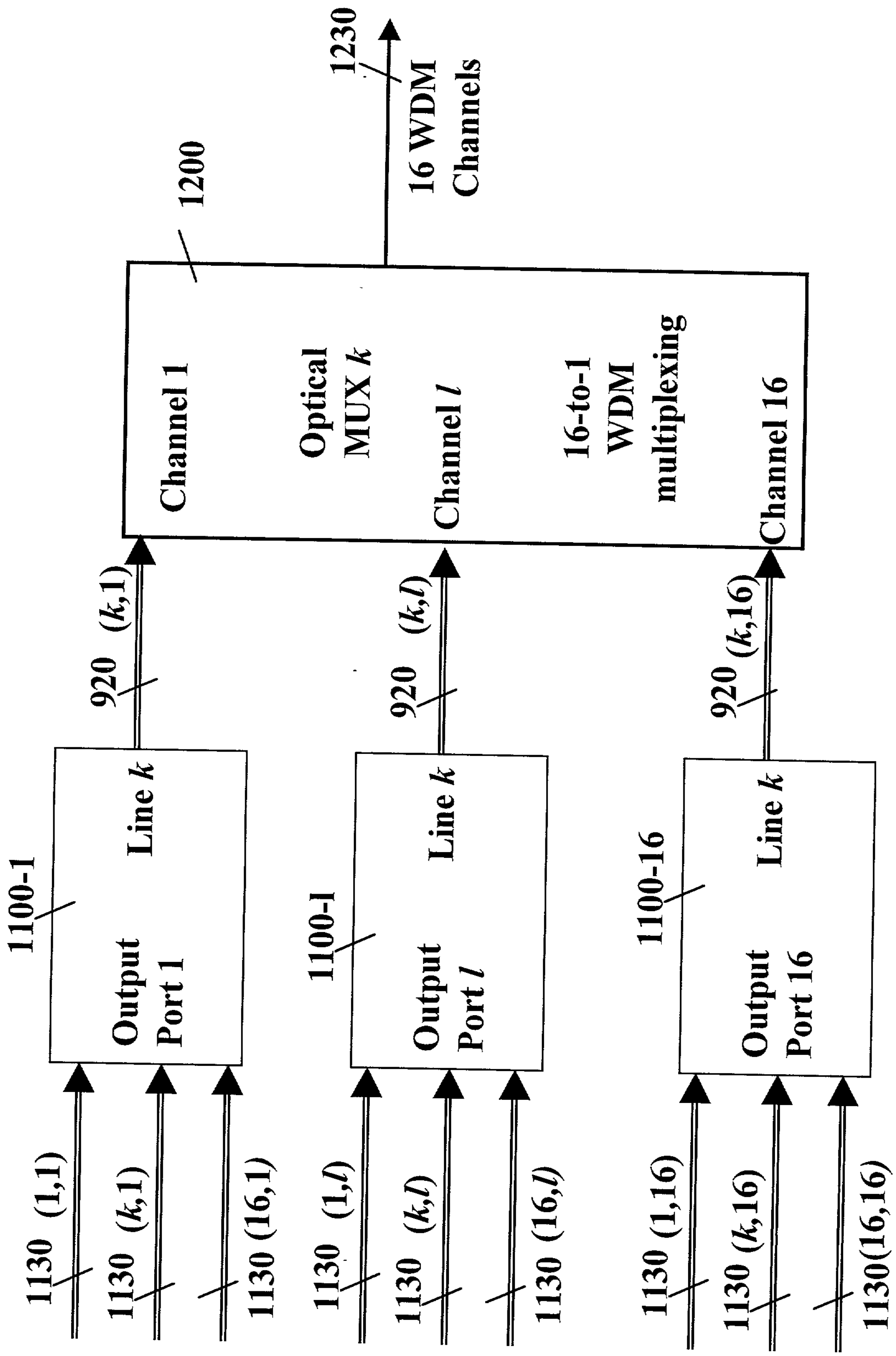

1230
16 WDM Channels
1200
Channel 1
Optical MUX k
Channel l
16-to-1 WDM multiplexing
Channel 16
920 (k,1)
920 (k,l)
920 (k,16)
1100-1
Line k
Output Port 1
1100-1
Line k
Output Port l
1100-16
Line k
Output Port 16
1130 (1,1)
1130 (k,1)
1130 (16,1)
1130 (1,l)
1130 (k,l)
1130 (16,l)
1130 (1,16)
1130 (k,16)
1130(16,16)

FIG. 16

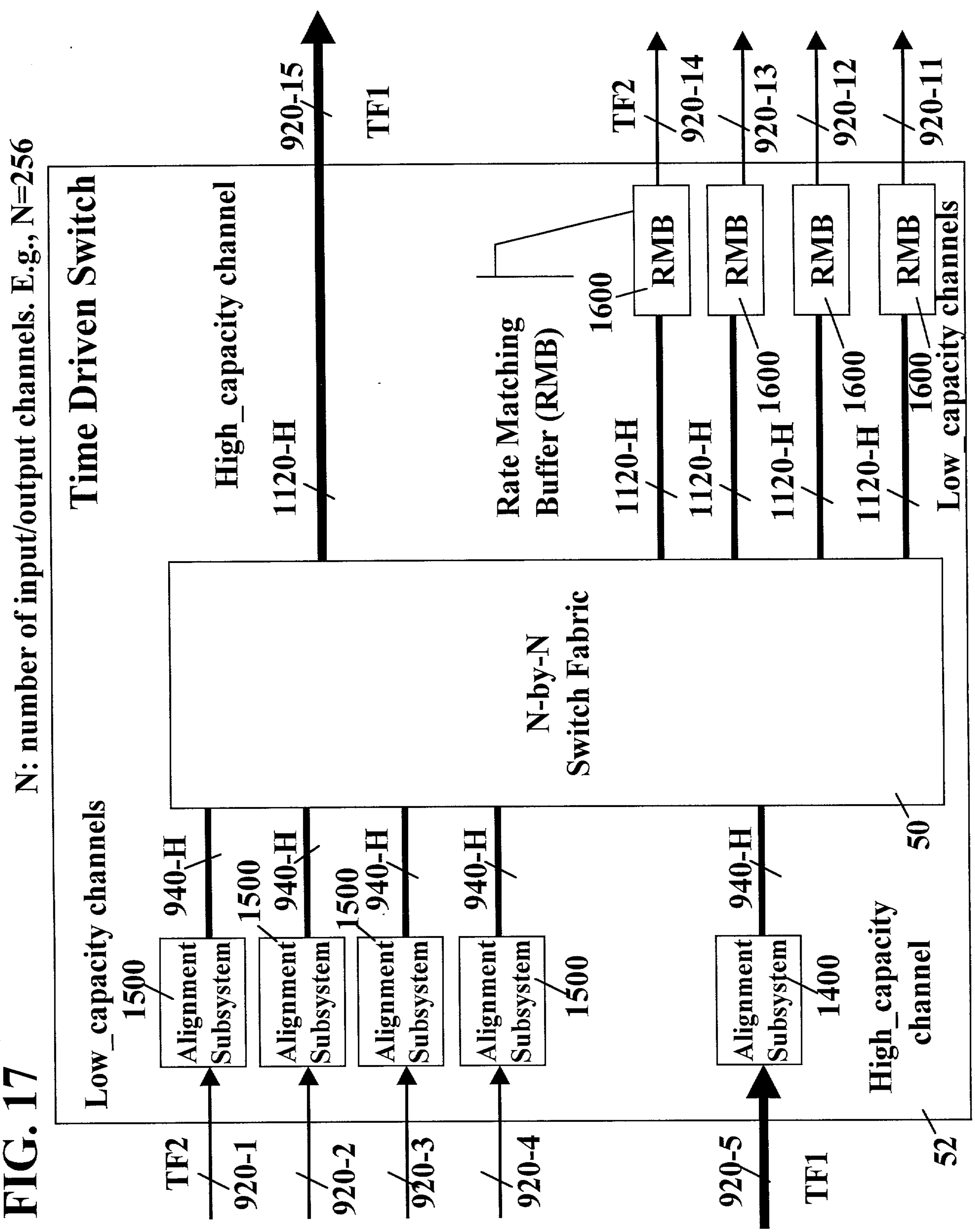
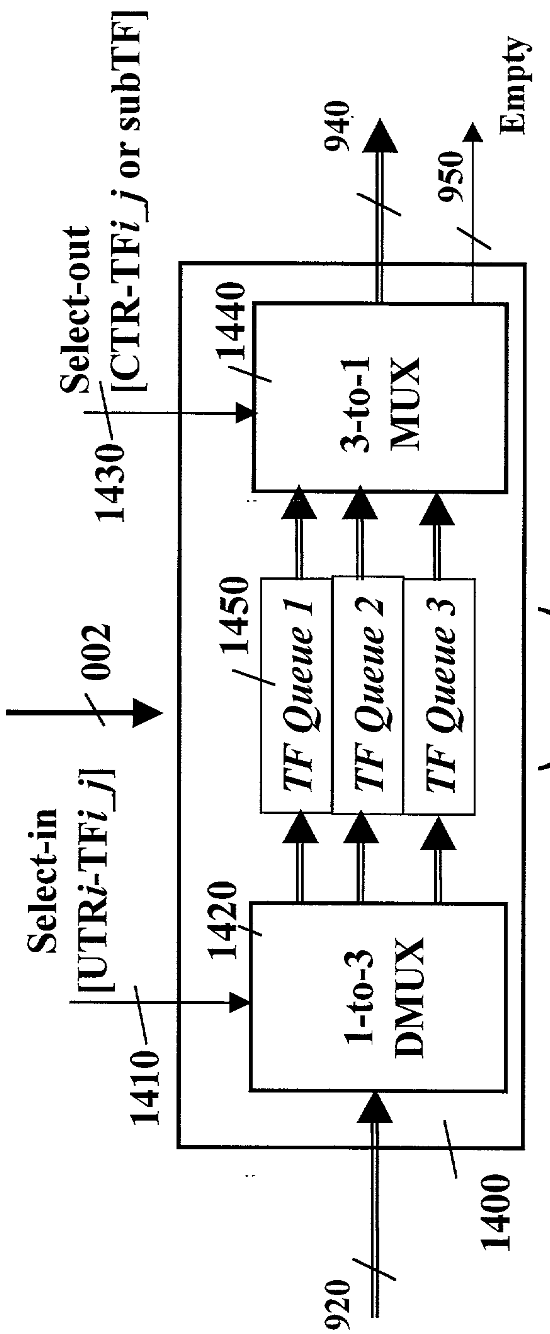

N: number of input/output channels. E.g., N=256
Time Driven Switch
Low_capacity channels
High_capacity channel
TF2
TF1
920-1
920-2
920-3
920-4
920-5
Alignment Subsystem
1500
1400
940-H
N-by-N Switch Fabric
50
52
1120-H
Rate Matching Buffer (RMB)
RMB
1600
920-11
920-12
920-13
920-14
920-15

FIG. 17

FIG. 18

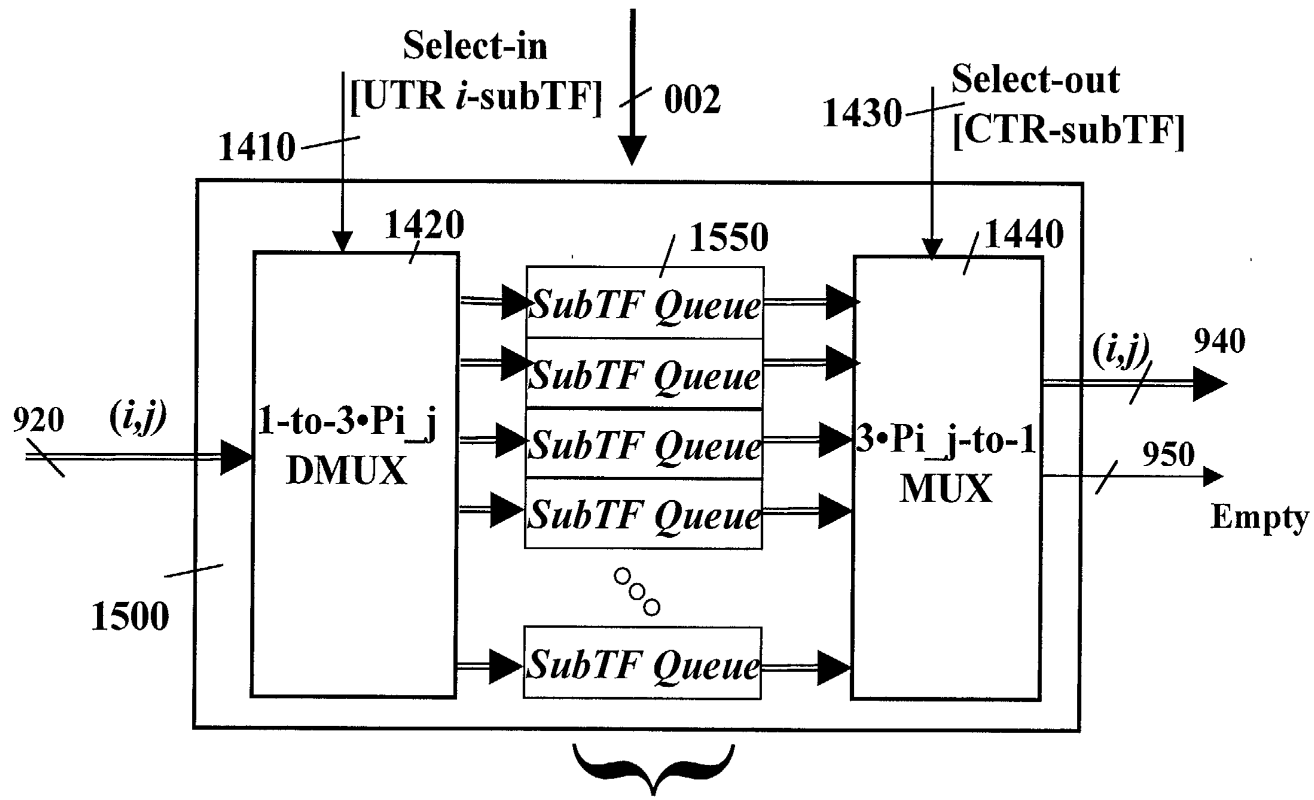
TF*i*_*j*: Time frame duration on channel *j* at Input Interface *i*.
UTR*i*: UTR on link connected to Input Interface *i*
Common Time Reference - CTR/UTC



Alignment Subsystem for Channel *j* at Input Interface *i*
with a Plurality of <u>Time Frame Queues</u>

FIG. 19

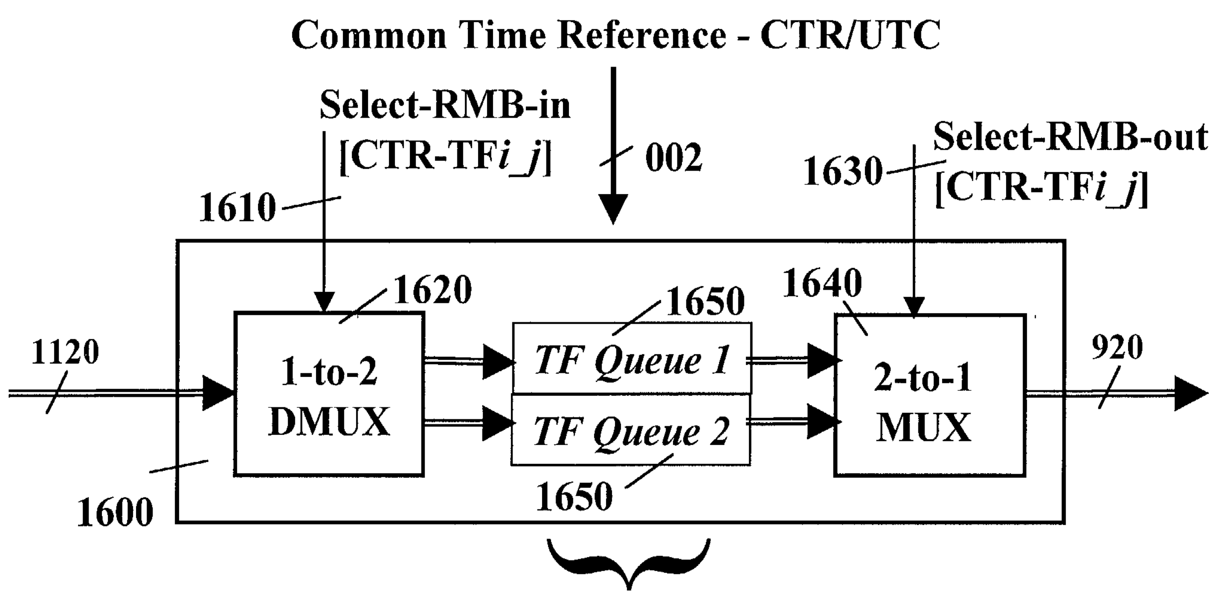
TF*i_j*: Time frame duration on channel *j* at Input Interface *i*.
UTR *i*: UTR on link connected to Input Interface *i*
P*i_j* = TF*i_j*/subTF



Alignment Subsystem for *high capacity* Channel *j* at Input Interface *i*
with a Plurality of <u>Sub-Time Frame Queues</u>

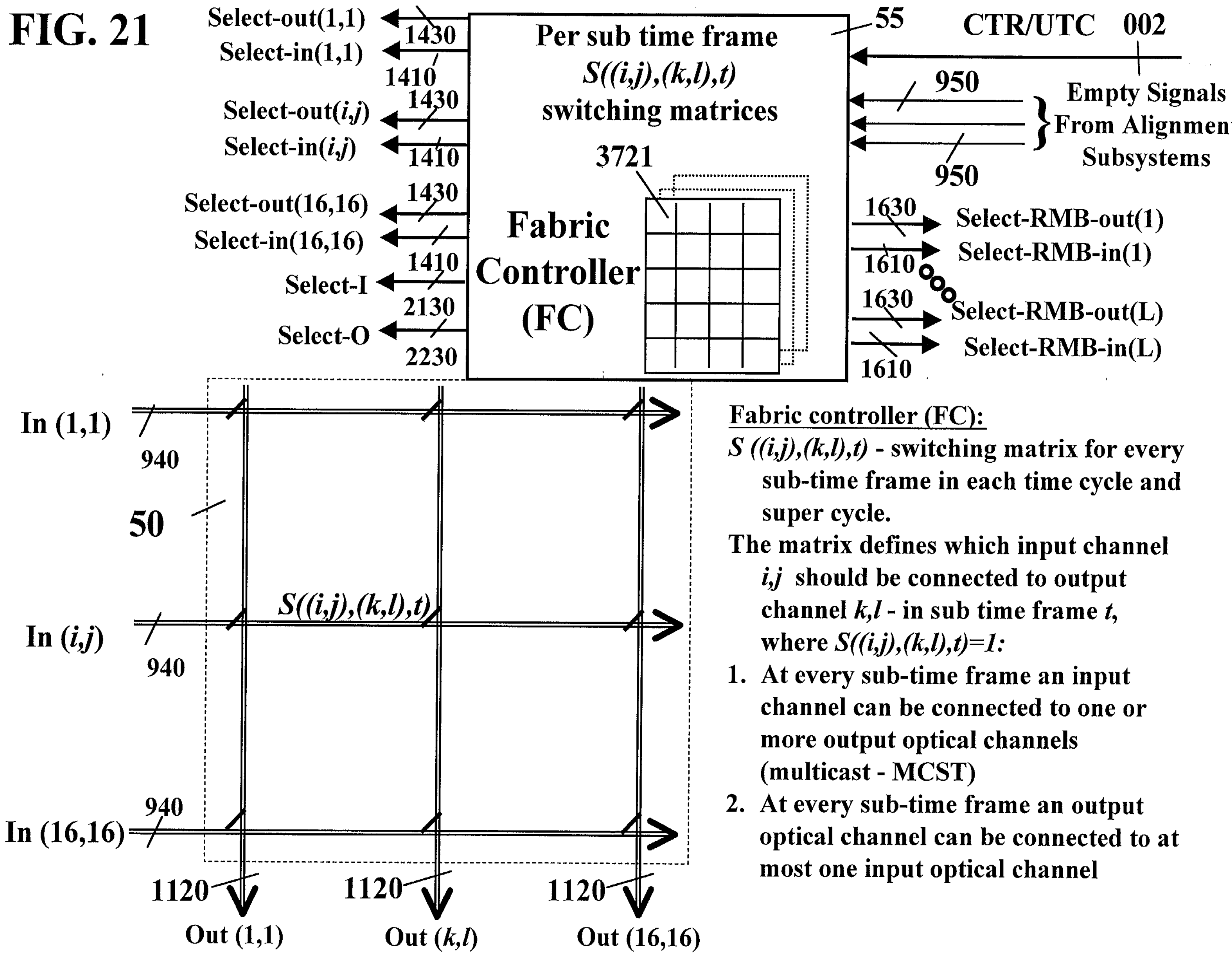
FIG. 20

TF*i_j*: Time frame duration on channel *j* at Input Interface *i*.
UTR*i*: UTR on link connected to Input Interface *i*



Rate Matching Buffer for Channel *j* at Output Interface *i*
with a Plurality of <u>Time Frame Queues</u>
(Also single buffer with dual access memory with single phase switching and forwarding)

FIG. 21



<u>Fabric controller (FC):</u>

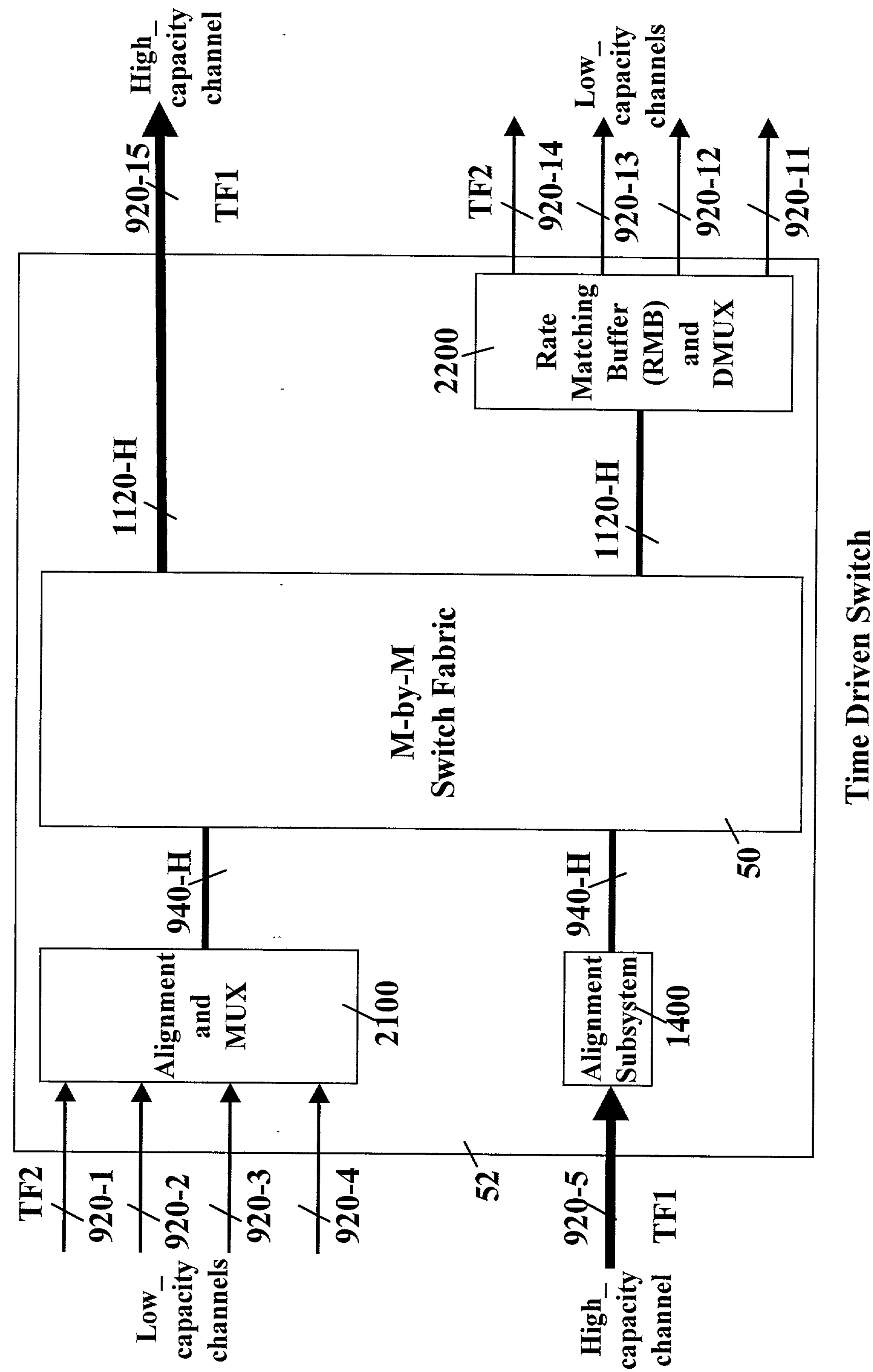
S ((i,j),(k,l),t) - switching matrix for every sub-time frame in each time cycle and super cycle.

The matrix defines which input channel *i,j* should be connected to output channel *k,l* - in sub time frame *t*, where *S((i,j),(k,l),t)=1:*

1. At every sub-time frame an input channel can be connected to one or more output optical channels (multicast - MCST)
2. At every sub-time frame an output optical channel can be connected to at most one input optical channel

FIG. 22

N: number of input/output channels. E.g., N=256
M • High_capacity = N_high • High_capacity + N_low • Low_capacity
M<N



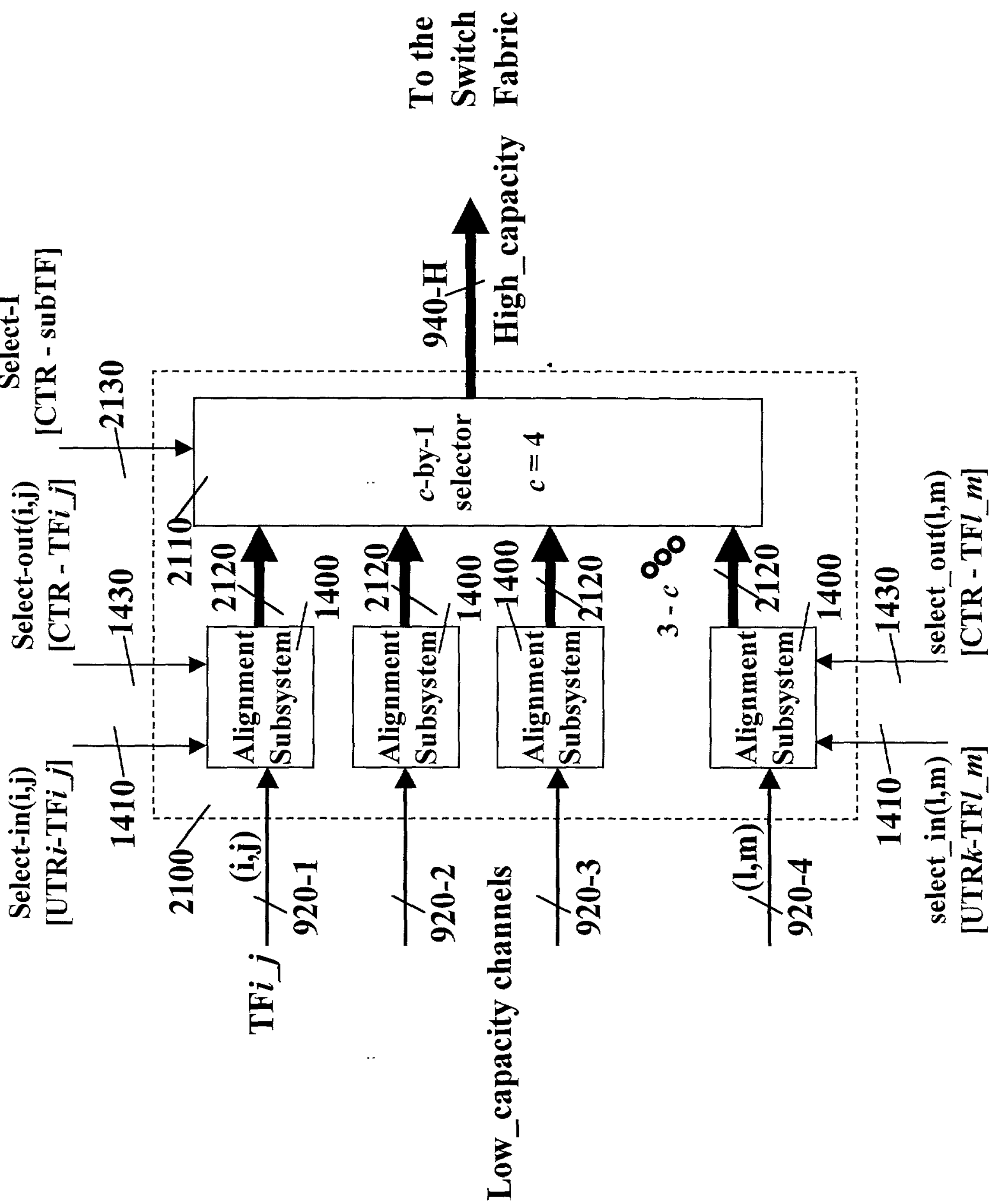

Select-in(i,j)
[UTRi-TFi_j]
1410
Select-out(i,j)
[CTR - TFi_j]
1430
Select-I
[CTR - subTF]
2130
2100
2110
c-by-1
selector
c = 4
2120
1400
Alignment Subsystem
3 - c
940-H
High_capacity
To the Switch Fabric
TFi_j
(i,j)
920-1
920-2
920-3
(l,m)
920-4
Low_capacity channels
select_in(l,m)
[UTRk-TFl_m]
select_out(l,m)
[CTR - TFl_m]

FIG. 23

FIG. 24

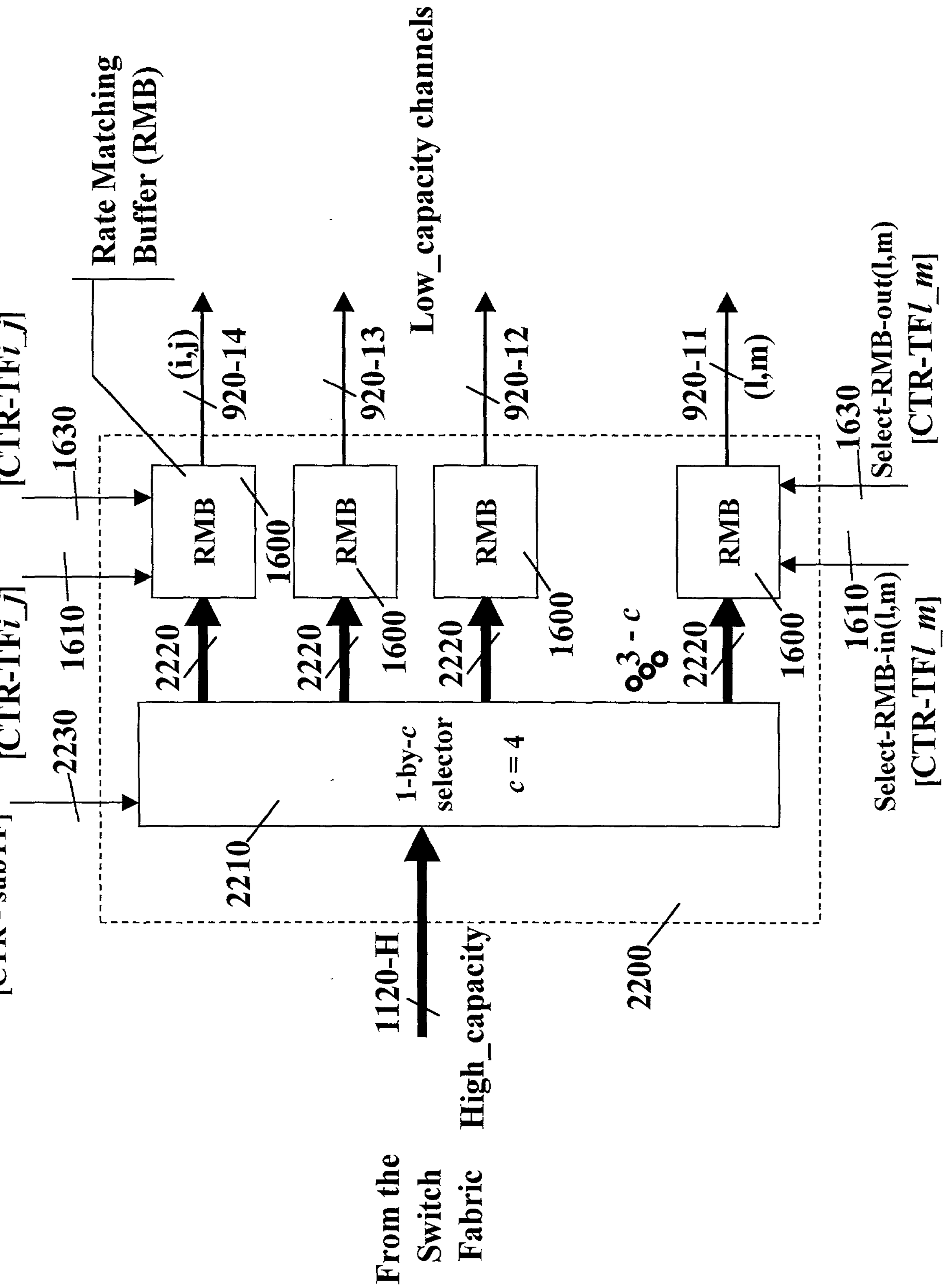

Rate Matching Buffer (RMB)
Low_capacity channels
Select-RMB-out(i,j) [CTR-TFi_j]
1630
Select-RMB-in(i,j) [CTR-TFi_j]
1610
Select-O [CTR - subTF]
2230
RMB
RMB
RMB
RMB
1600
1600
1600
1600
2220
2220
2220
2220
(i,j)
920-14
920-13
920-12
920-11
(l,m)
3 - c
1-by-c selector
c = 4
2210
1120-H
High_capacity
From the Switch Fabric
2200
1630
Select-RMB-out(l,m) [CTR-TFl_m]
1610
Select-RMB-in(l,m) [CTR-TFl_m]

FIG. 25

N: number of input/output channels. E.g., N=256
L • Low_capacity = N_high • High_capacity + N_low • Low_capacity
L > N

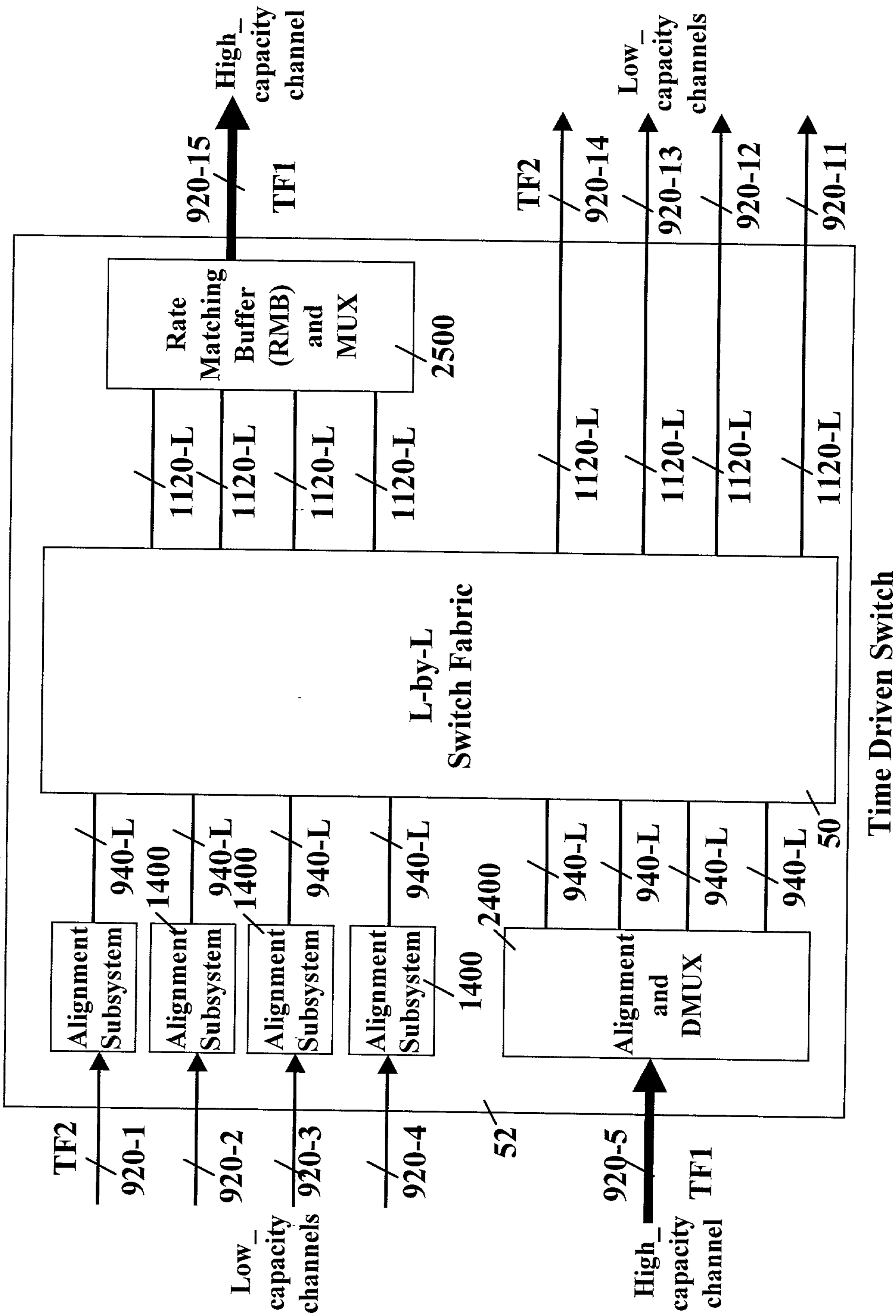
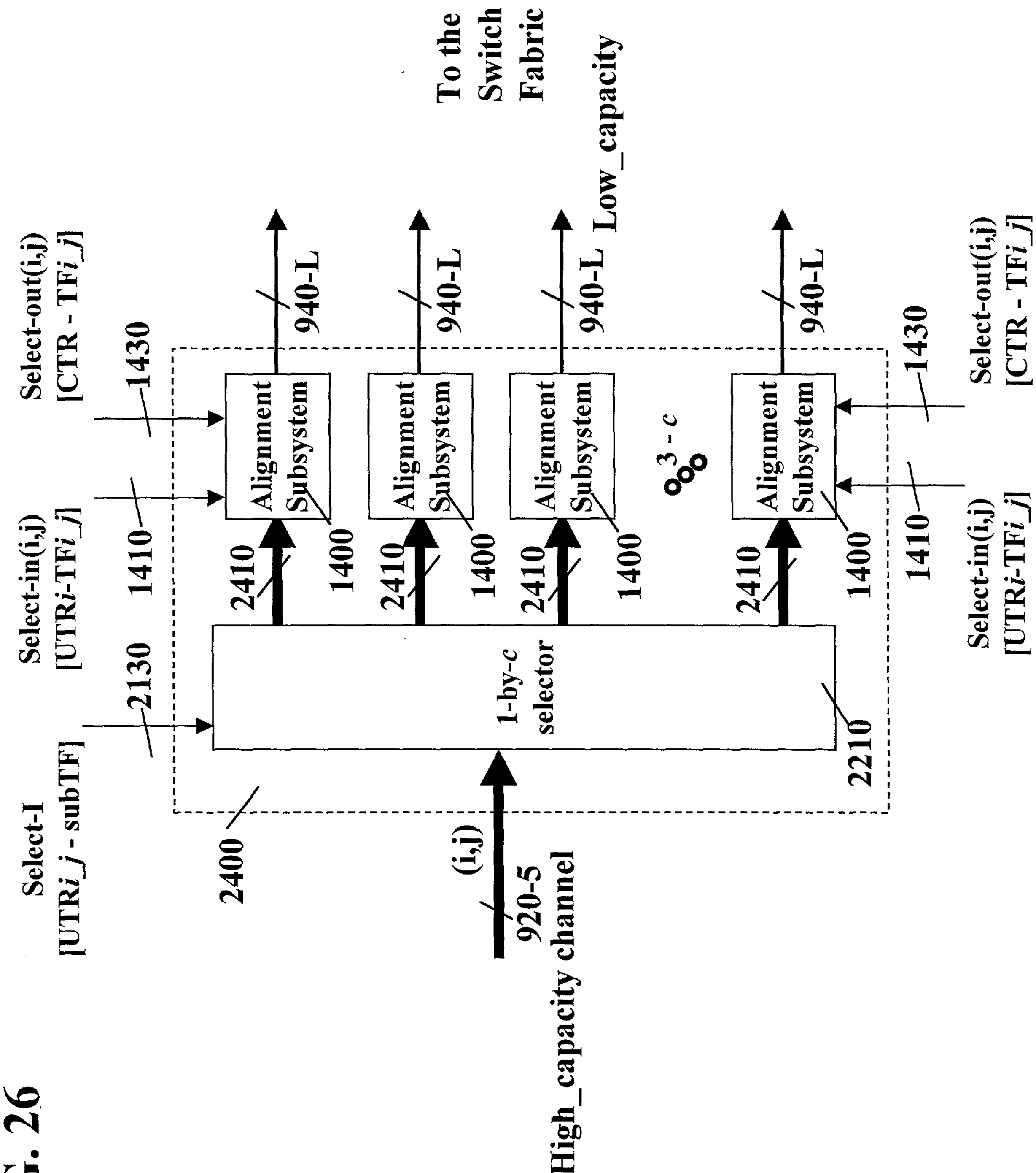


FIG. 26


Select-I
[UTRi_j - subTF]
2130
Select-in(i,j)
[UTRi-TFi_j]
1410
Select-out(i,j)
[CTR - TFi_j]
1430
2400
(i,j)
920-5
High_capacity channel
1-by-c
selector
2210
2410
Alignment
Subsystem
1400
940-L
3 - c
To the
Switch
Fabric
Low_capacity

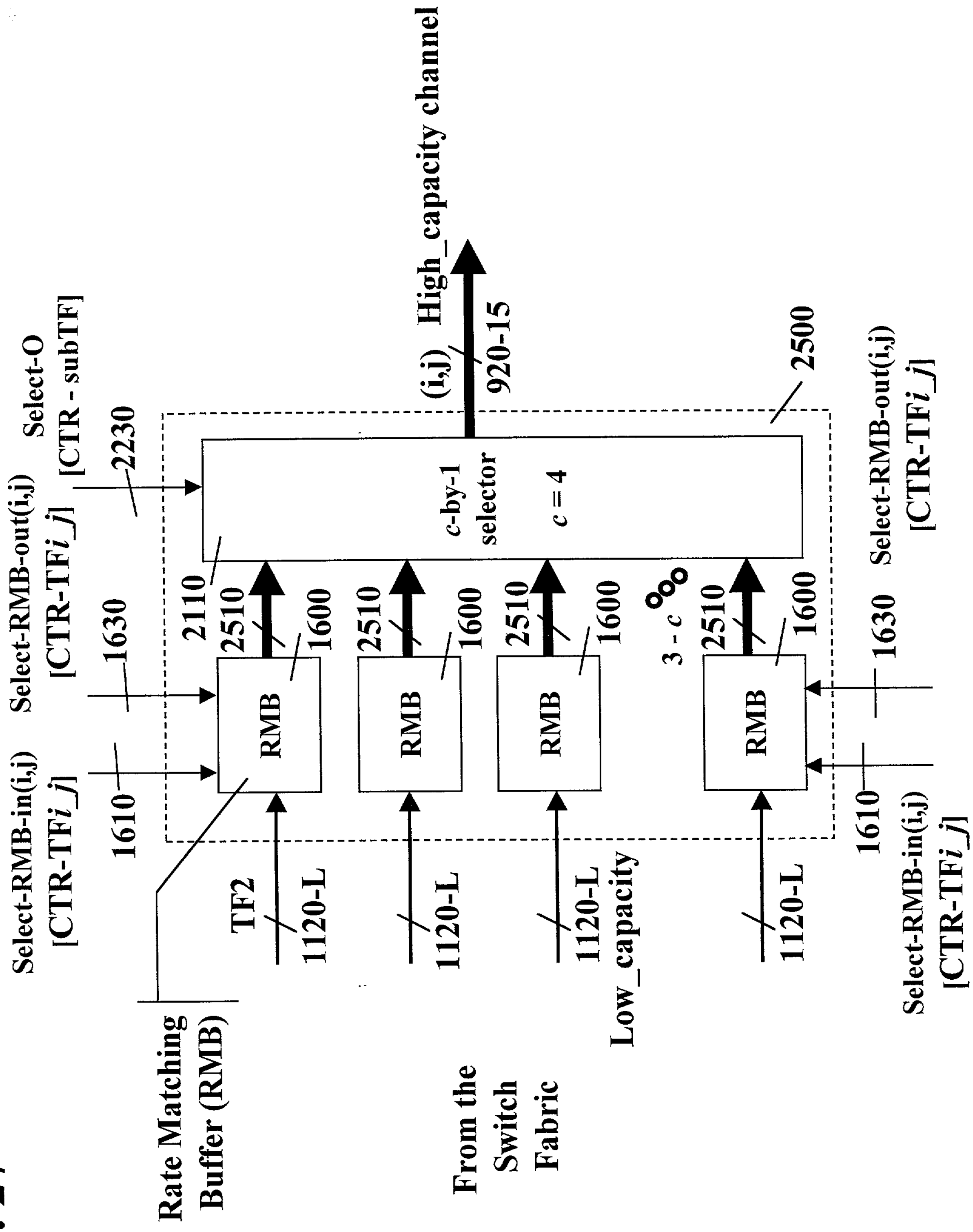
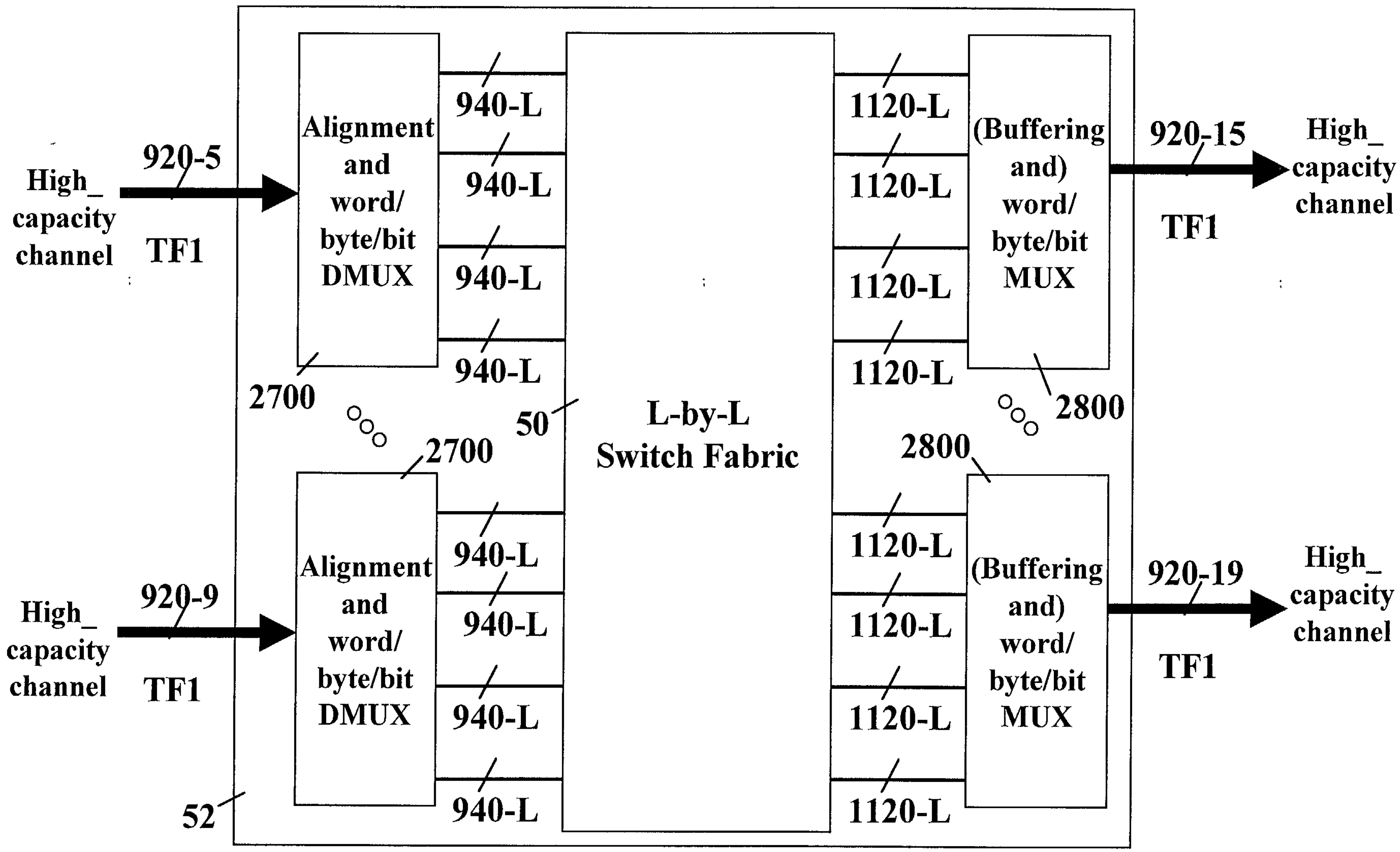

High_capacity channel
(i,j)
920-15
2500
Select-O
[CTR - subTF]
2230
Select-RMB-out(i,j)
[CTR-TFi_j]
1630
Select-RMB-in(i,j)
[CTR-TFi_j]
1610
c-by-1
selector
c = 4
2110
2510
1600
RMB
3 - c
TF2
1120-L
Low_capacity
Rate Matching
Buffer (RMB)
From the
Switch
Fabric

FIG. 27

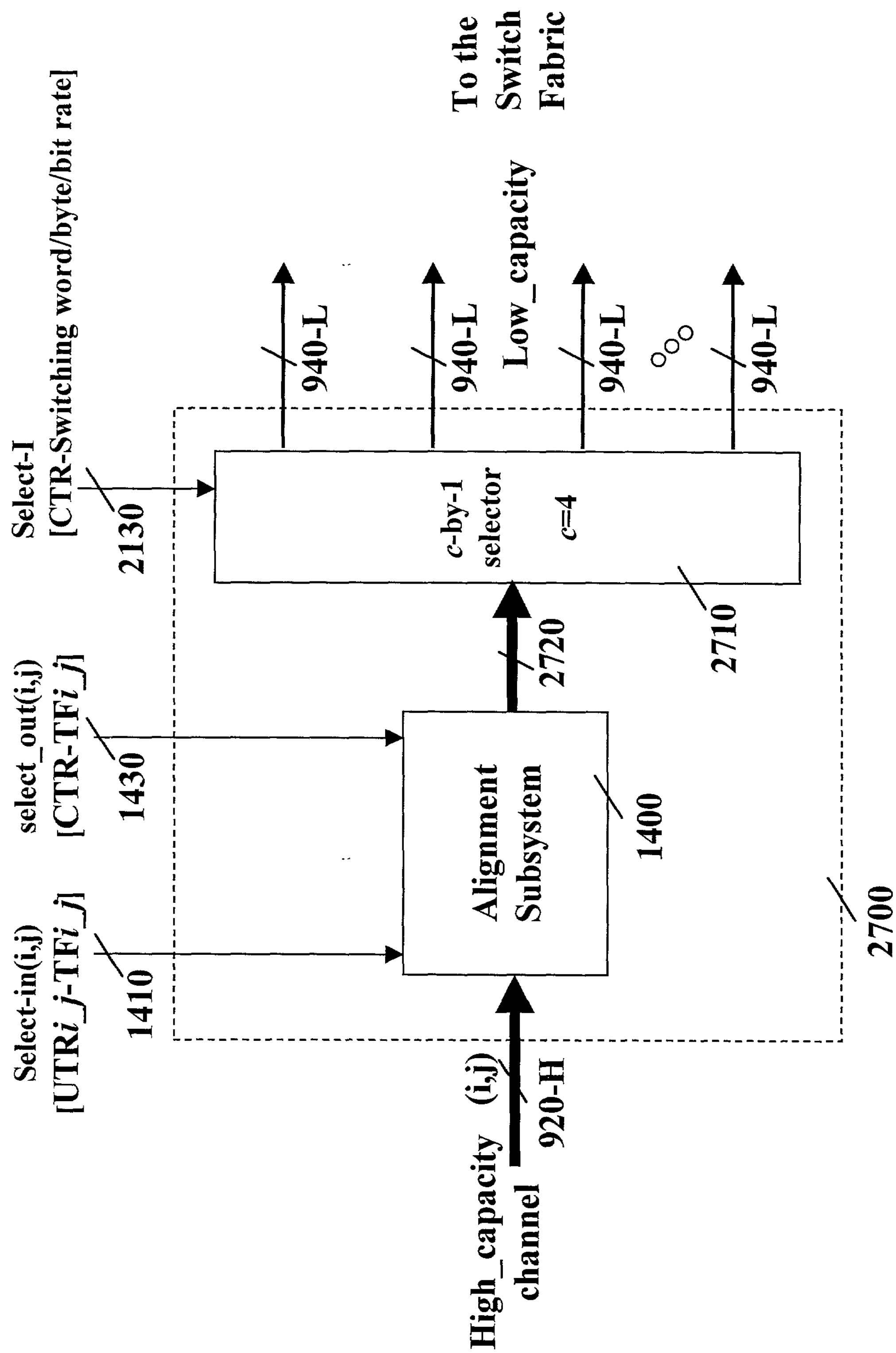
FIG. 28

N: number of input/output channels. E.g., N=256
L • Low_capacity = N • High_capacity
L = c • N > N



Time Driven Switch

FIG. 29


Select-in(i,j)
[UTRi_j-TFi_j]
1410
select_out(i,j)
[CTR-TFi_j]
1430
Select-I
[CTR-Switching word/byte/bit rate]
2130
High_capacity (i,j)
channel
920-H
Alignment
Subsystem
1400
2720
c-by-1
selector
c=4
2710
2700
940-L
940-L
940-L
940-L
Low_capacity
To the
Switch
Fabric

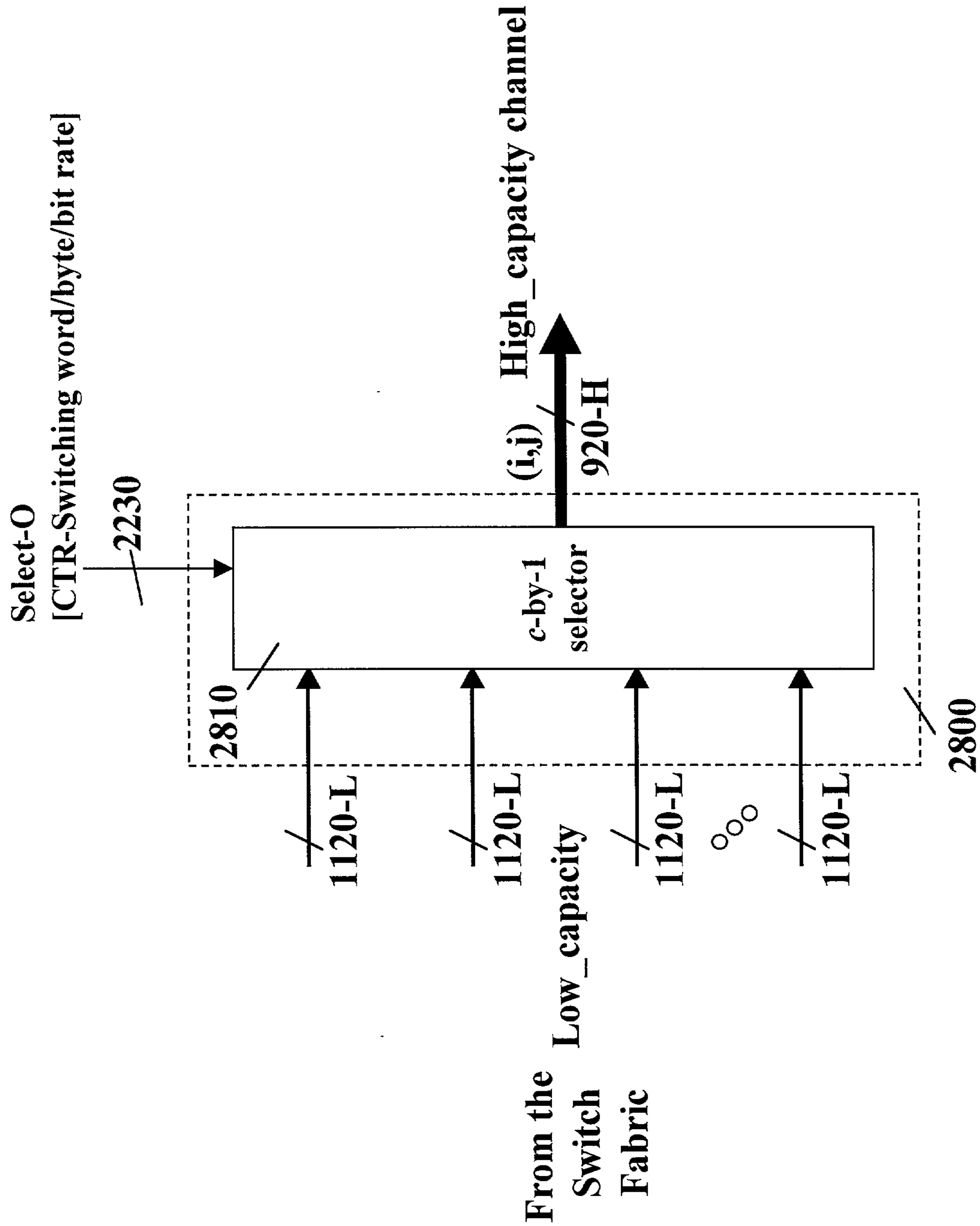

Select-O
[CTR-Switching word/byte/bit rate]
2230
(i,j)
High_capacity channel
920-H
c-by-1
selector
2810
2800
1120-L
1120-L
1120-L
1120-L
From the
Switch
Fabric
Low_capacity

FIG. 30

FIG. 31

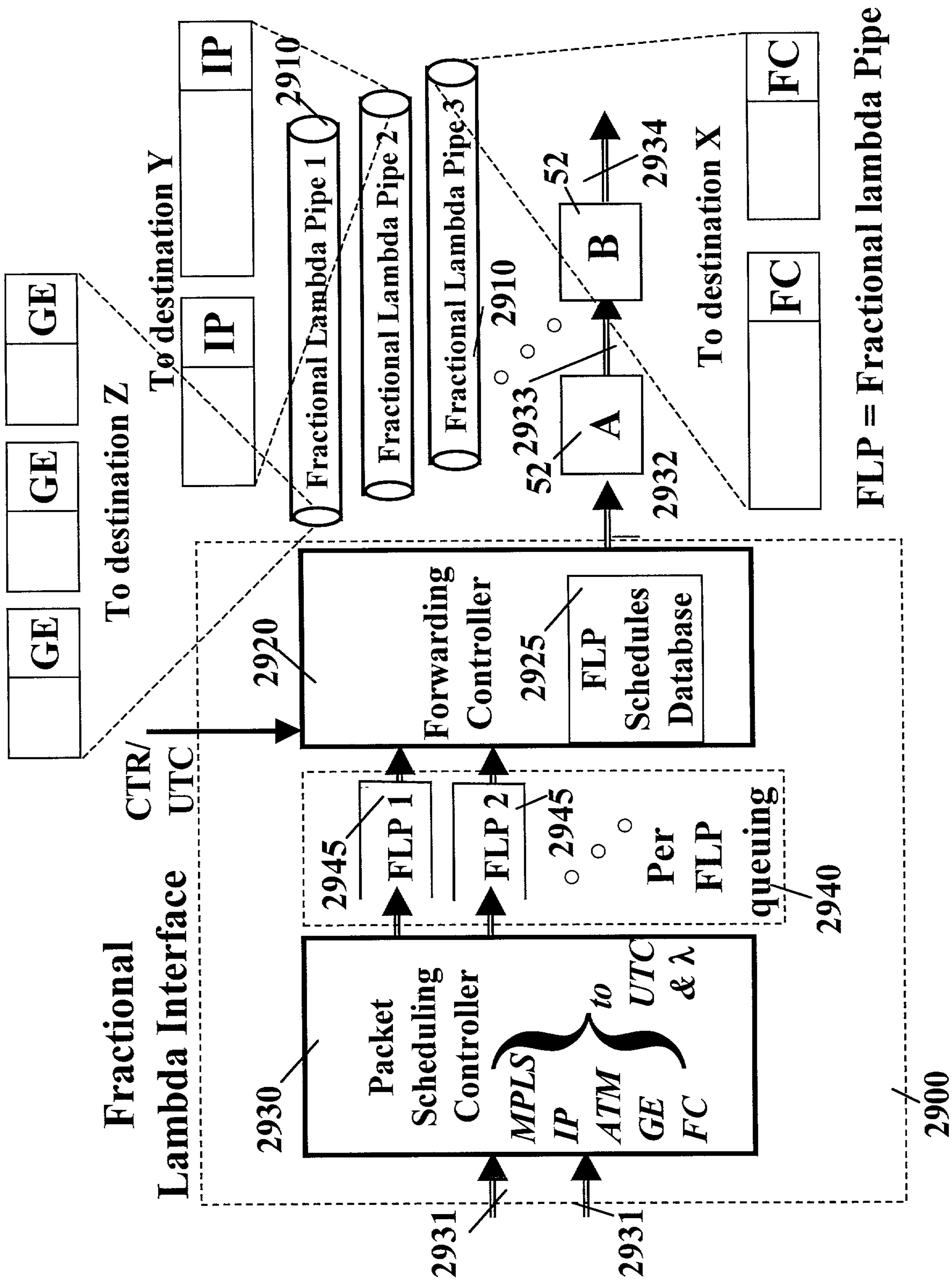

Fractional Lambda Interface
Packet Scheduling Controller
MPLS IP ATM GE FC
to UTC & λ
2930
2931
2931
2900
FLP 1
FLP 2
2945
2945
Per FLP queuing
2940
CTR/UTC
2920
Forwarding Controller
2925
FLP Schedules Database
2932
A
B
52
52
2933
2934
Fractional Lambda Pipe 1
Fractional Lambda Pipe 2
Fractional Lambda Pipe 3
2910
2910
To destination Z
GE
GE
GE
To destination Y
IP
IP
To destination X
FC
FC
FLP = Fractional lambda Pipe

FIG. 32

Channel Capacity		TF Duration	TF Size		STS-1s	TFs/s
51.84	STS- 1	250	1620	1512	2	4000
		500	3240	3024	4	2000
		1000	6480	6048	8	1000
155.52	STS- 3	125	2430	2268	3	8000
		250	4860	4536	6	4000
		500	9720	9072	12	2000
622.08	STS- 12	62.5	4860	4536	6	16000
		125	9720	9072	12	8000
		250	19440	18144	24	4000
2488.32	STS- 48	62.5	19440	18144	24	16000
		31.25	9720	9072	12	32000
		15.625	4860	4536	6	64000
9953.28	STS- 192	7.8125	9720	9072	12	128000
		15.625	19440	18144	24	64000
1000	GE	125	15625	15625	19.3	8000
		100	12500	12500	15.4	10000
		80	10000	10000	12.3	12500
10000	10GE	15.625	19531.25	19531.3	24.1	64000
		12.5	15625	15625	19.3	80000
		10	12500	12500	15.4	100000

FIG. 33

Ch Capacity		TF Dur.	TF Size	GE TFs	TFs/s
1000	**GE**	**80**	**10000**	**1.0**	**12500**
51.84	STS- 1	250	1512	0.15	4000
		500	3024	0.30	2000
		1000	6048	0.60	1000
155.5	STS- 3	125	2268	0.23	8000
		250	4536	0.45	4000
		500	9072	0.91	2000
622.1	STS- 12	62.5	4536	0.45	16000
		125	9072	0.91	8000
		250	18144	1.81	4000
2488	STS- 48	62.5	18144	1.81	16000
		31.25	9072	0.91	32000
		15.625	4536	0.45	64000
9953	STS- 192	7.8125	9072	0.91	128000
		15.625	18144	1.81	64000
10000	10GE	8	10000	1.00	125000
		16	20000	2.00	62500

FIG. 34

Ch Capacity		TF Dur.	TF Size	GE TFs	TFs/s
1000	**GE**	**62.5**	**7812.5**	**1.0**	**16000**
51.84	STS- 1	250	1512	0.19	4000
		500	3024	0.39	2000
		1000	6048	0.77	1000
155.52	STS- 3	125	2268	0.29	8000
		250	4536	0.58	4000
		500	9072	1.16	2000
622.08	STS- 12	62.5	4536	0.58	16000
		125	9072	1.16	8000
		250	18144	2.32	4000
2488.32	STS- 48	62.5	18144	2.32	16000
		31.25	9072	1.16	32000
		15.625	4536	0.58	64000
9953.28	STS- 192	7.8125	9072	1.16	128000
		15.625	18144	2.32	64000
10000	10GE	12.5	15625	2.00	80000
		25	31250	4.00	40000

FIG. 35

TF Alignment of UTR(j) *to* UTC - with three input queues - principle of operation:

The same queue is not used simultaneously for:

1. Receiving data packets from the serial link, and

2. Forwarding data packets to the switch

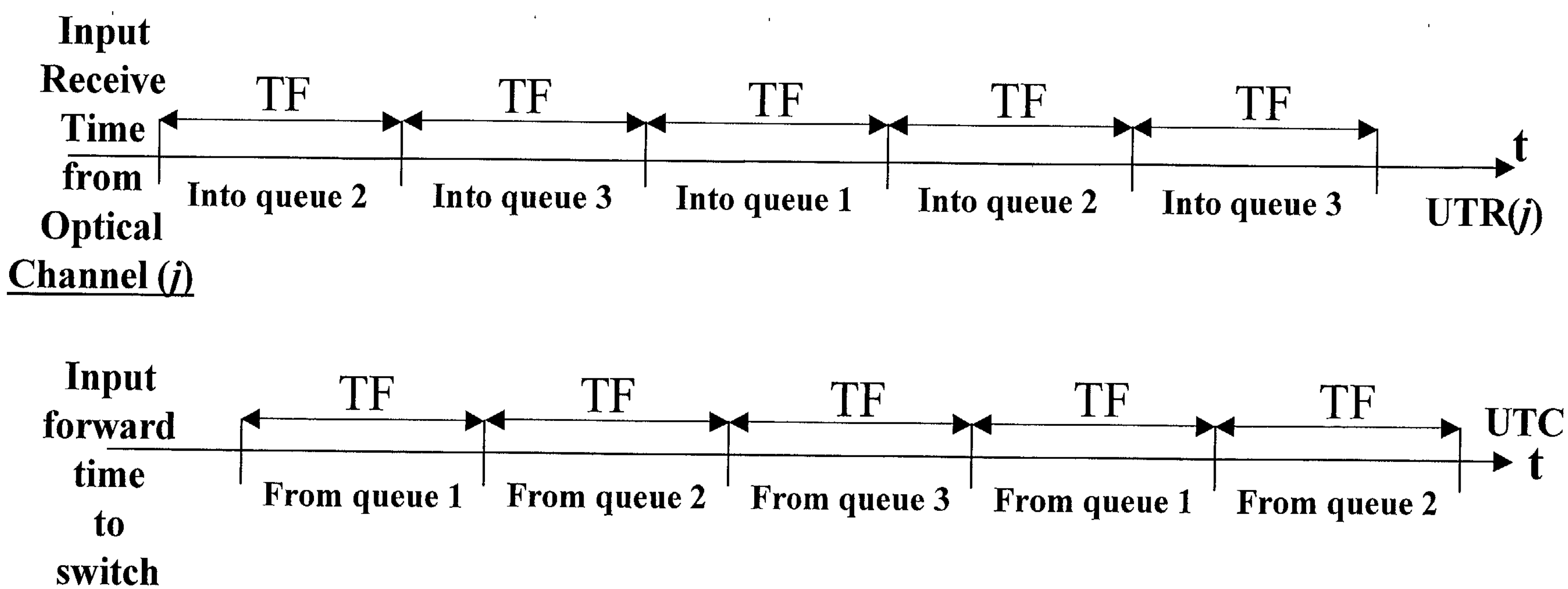


FIG. 36

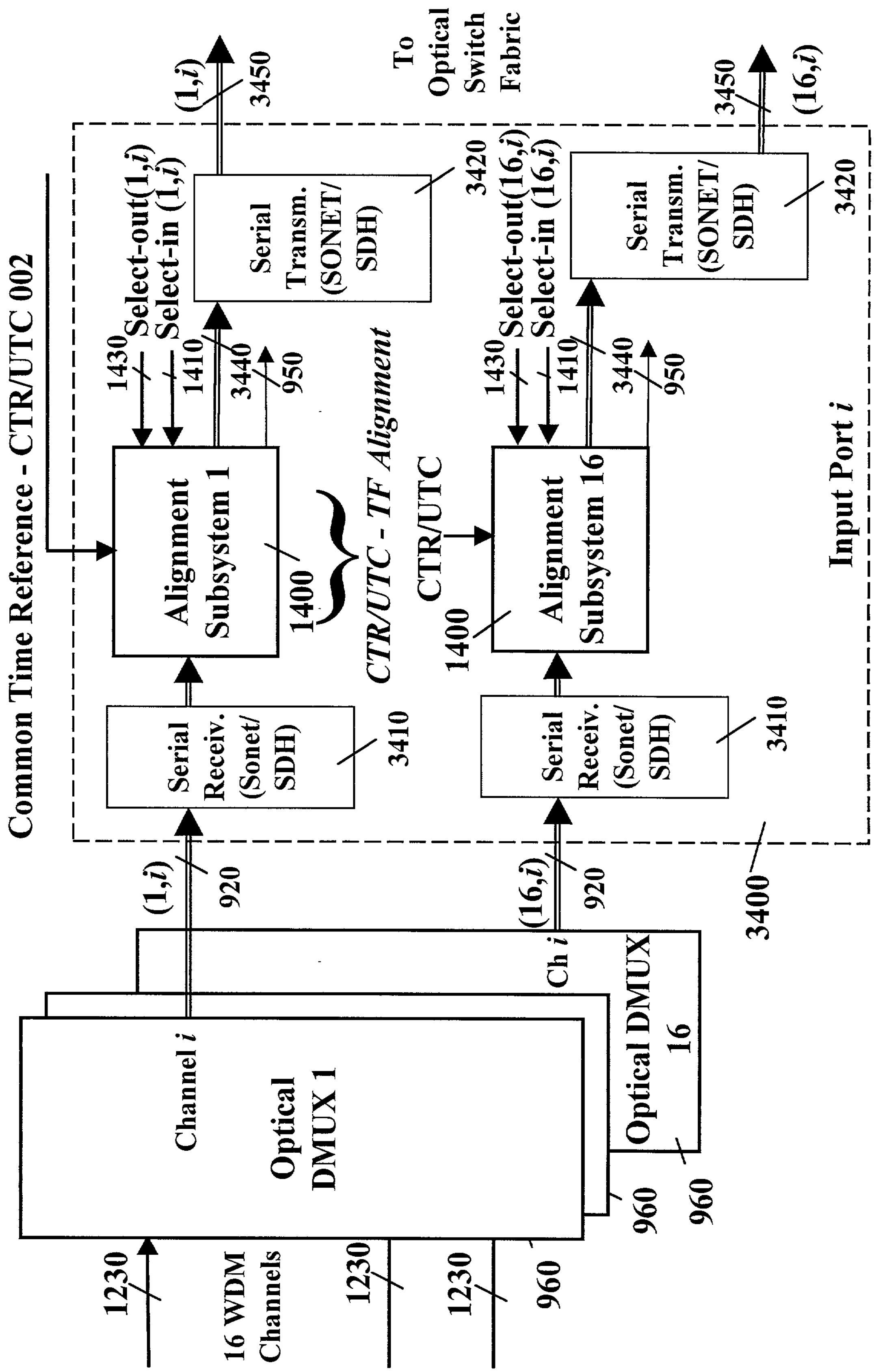

Common Time Reference - CTR/UTC 002
16 WDM Channels
1230
1230
1230
960
960
960
Optical DMUX 1
Channel i
Optical DMUX 16
Ch i
(1,i)
920
(16,i)
920
Serial Receiv. (Sonet/ SDH)
3410
Serial Receiv. (Sonet/ SDH)
3410
Alignment Subsystem 1
1400
Alignment Subsystem 16
1400
CTR/UTC - TF Alignment
CTR/UTC
1430
Select-out(1,i)
Select-in (1,i)
1410
3440
950
1430
Select-out(16,i)
Select-in (16,i)
1410
3440
950
Serial Transm. (SONET/ SDH)
3420
Serial Transm. (SONET/ SDH)
3420
(1,i)
3450
3450
(16,i)
To Optical Switch Fabric
Input Port i
3400

FIG. 37

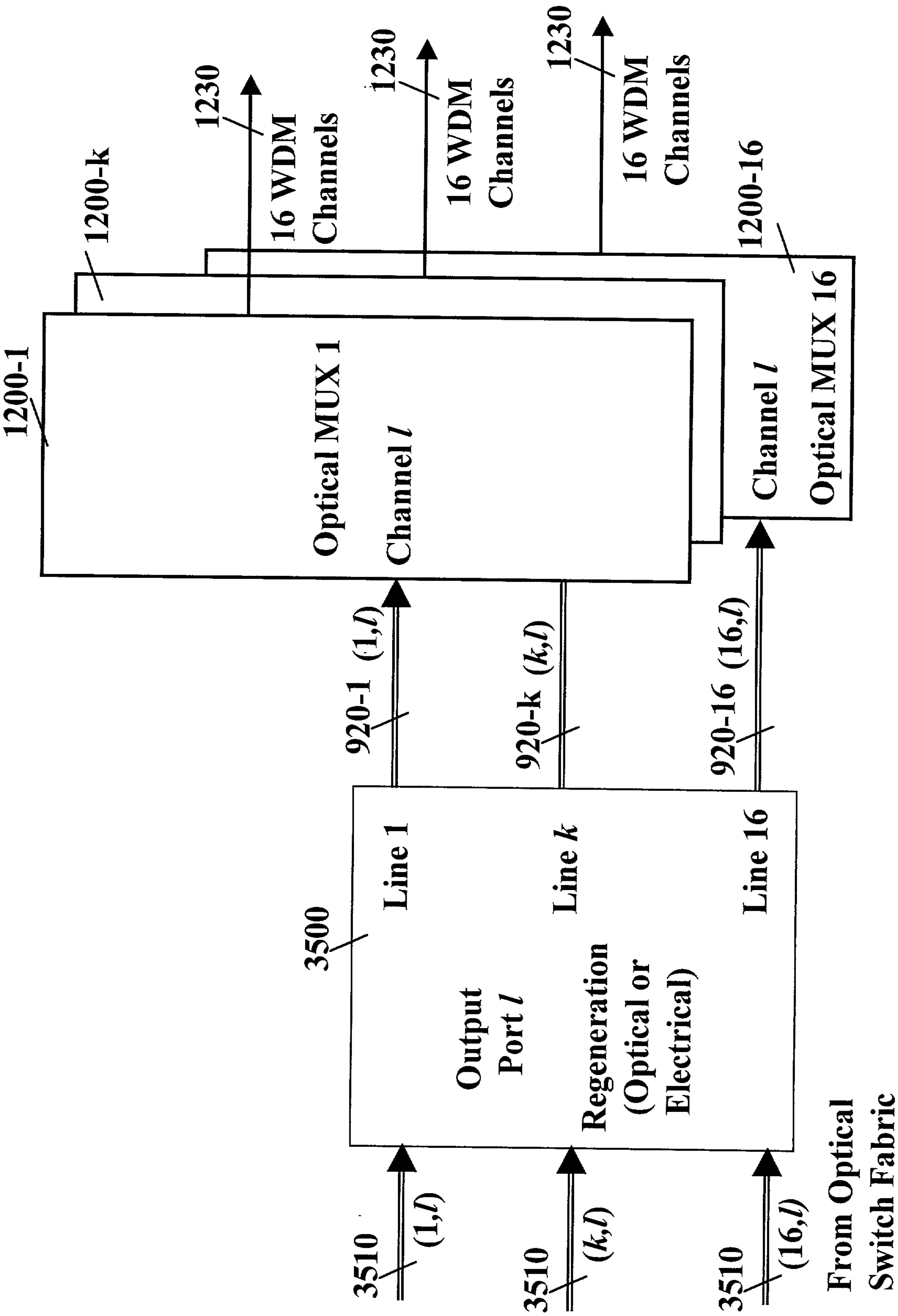

3510
(1,l)
3510
(k,l)
3510
(16,l)
From Optical Switch Fabric
3500
Output Port l
Regeneration (Optical or Electrical)
Line 1
Line k
Line 16
920-1 (1,l)
920-k (k,l)
920-16 (16,l)
1200-1
Optical MUX 1
Channel l
1200-k
1200-16
Channel l
Optical MUX 16
1230
16 WDM Channels
1230
16 WDM Channels
1230
16 WDM Channels

FIG. 38

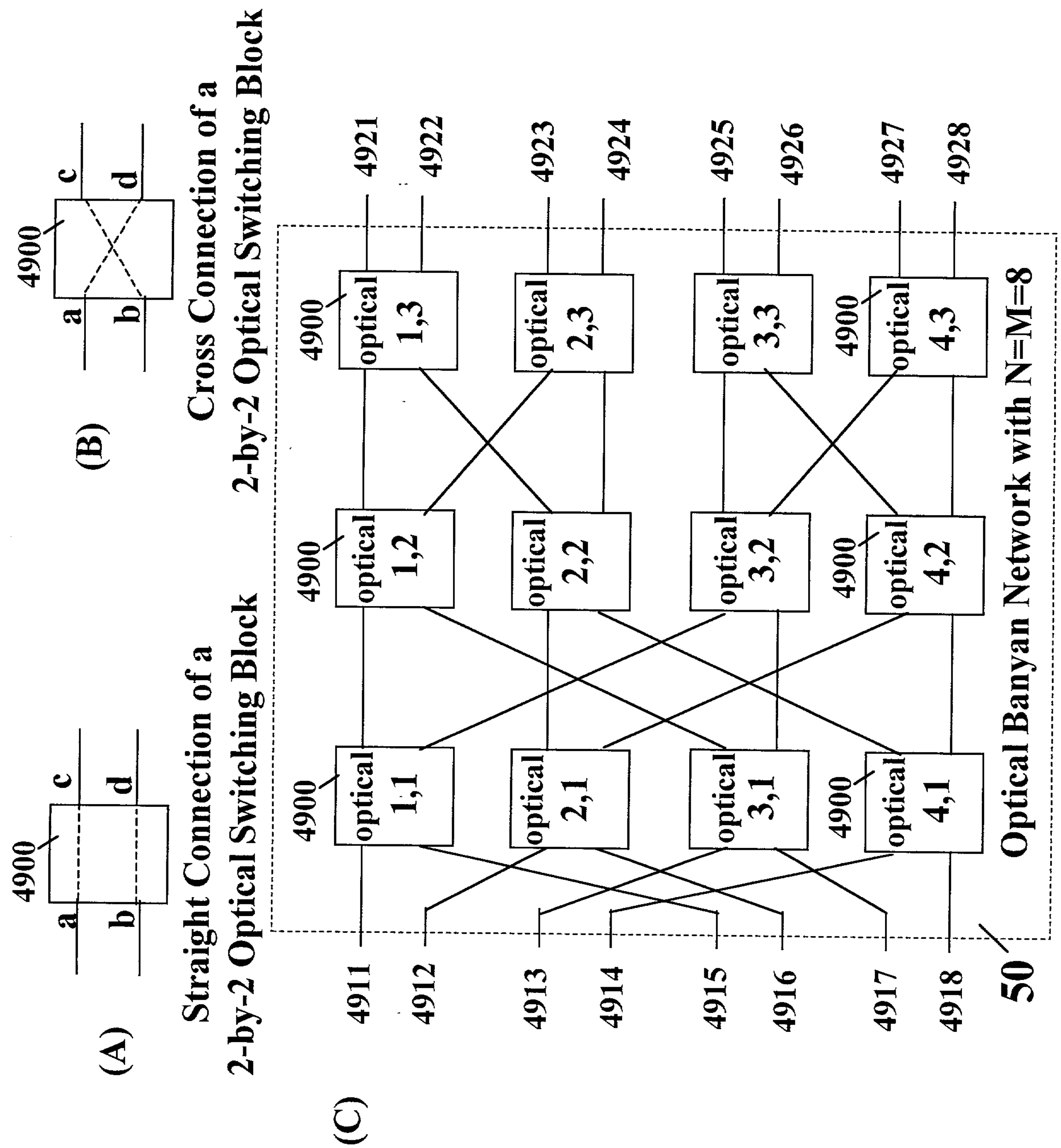
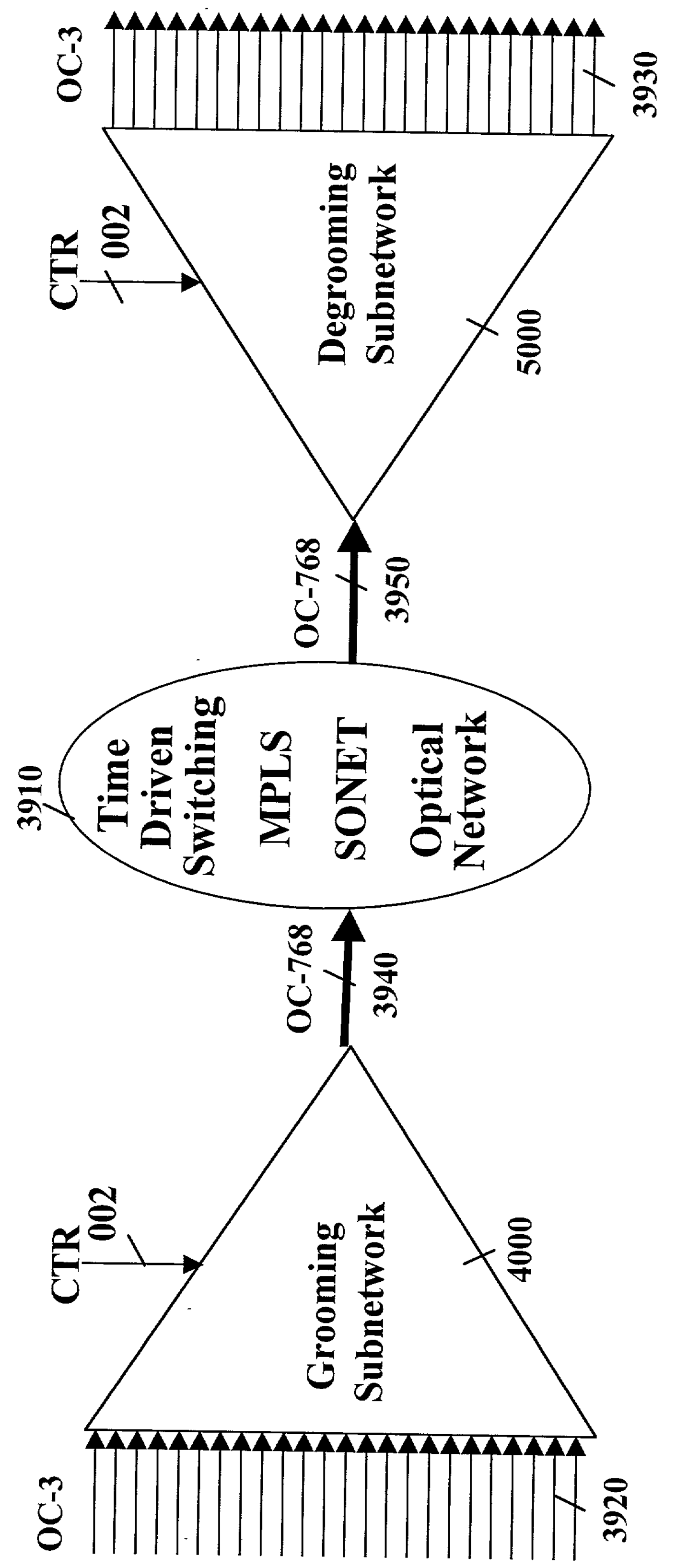

(A)
4900
a
b
c
d
Straight Connection of a
2-by-2 Optical Switching Block
(B)
4900
a
b
c
d
Cross Connection of a
2-by-2 Optical Switching Block
(C)
4911
4912
4913
4914
4915
4916
4917
4918
4900
optical 1,1
optical 2,1
optical 3,1
optical 4,1
optical 1,2
optical 2,2
optical 3,2
optical 4,2
optical 1,3
optical 2,3
optical 3,3
optical 4,3
4921
4922
4923
4924
4925
4926
4927
4928
50
Optical Banyan Network with N=M=8

FIG. 39


OC-3
3920
Grooming
Subnetwork
CTR
002
4000
OC-768
3940
3910
Time
Driven
Switching
MPLS
SONET
Optical
Network
OC-768
3950
Degrooming
Subnetwork
CTR
002
5000
OC-3
3930

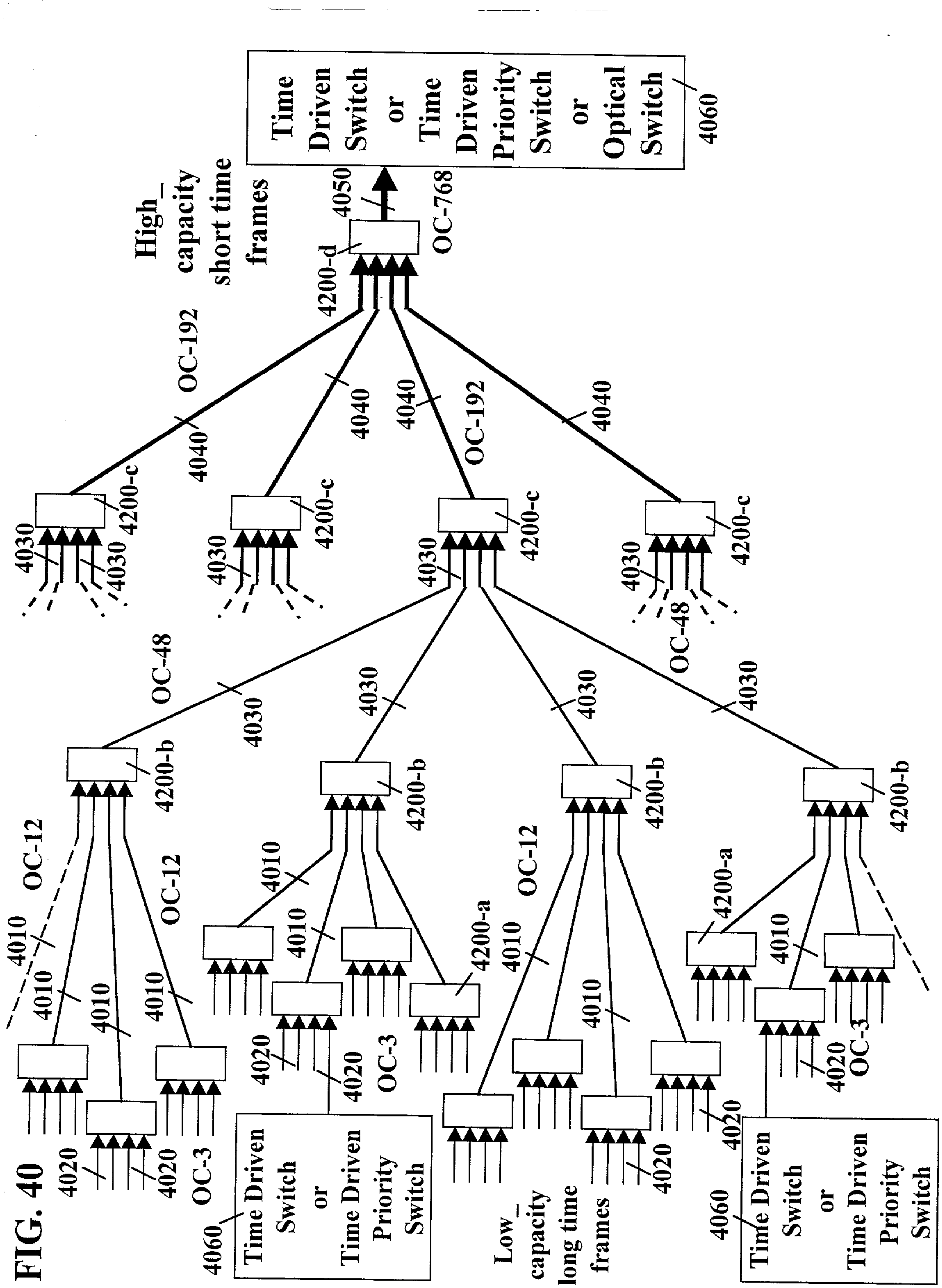
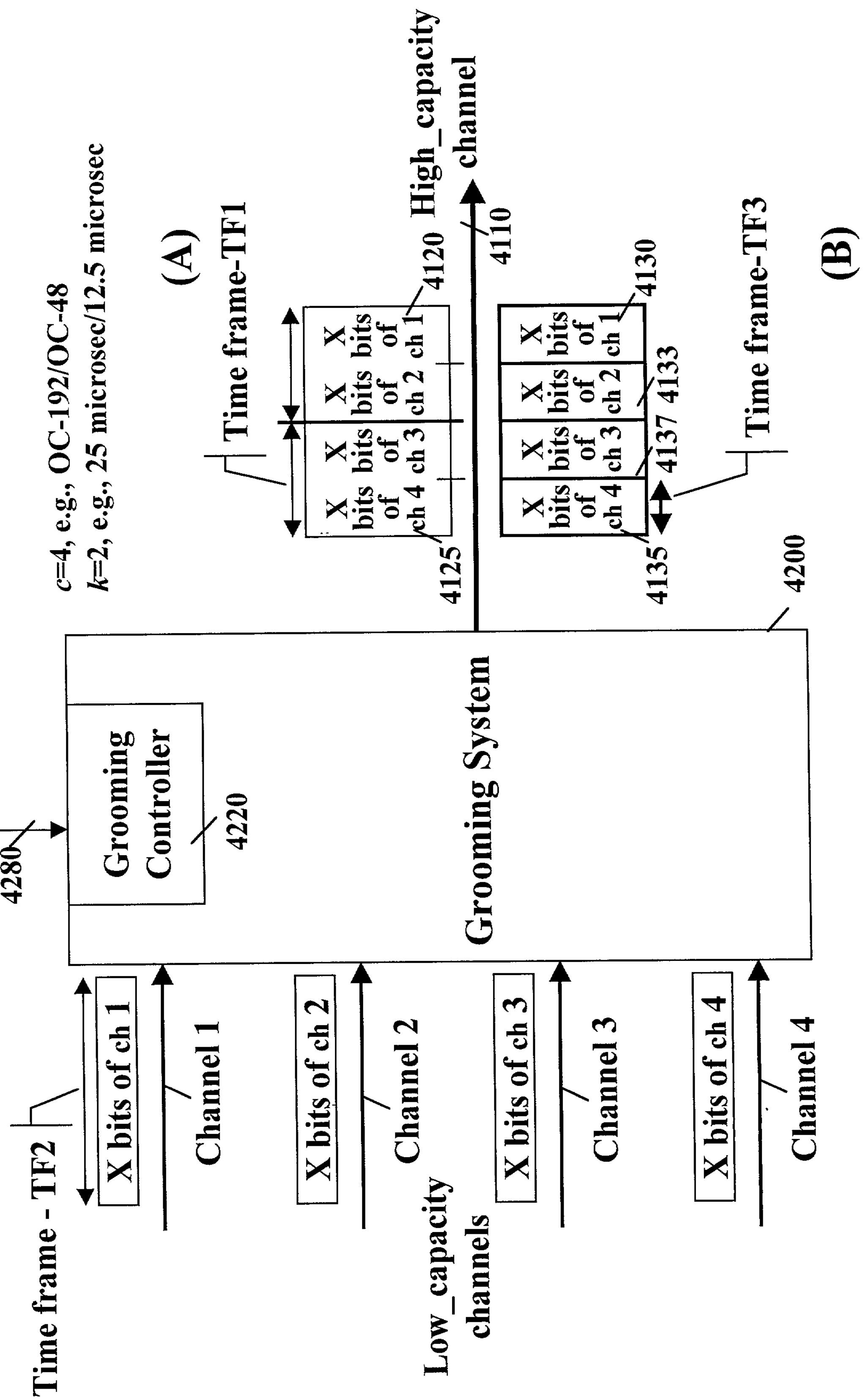

Time Driven Switch or Time Driven Priority Switch or Optical Switch
4060
High_ capacity short time frames
4050
OC-768
4200-d
OC-192
4040
4200-c
4030
OC-48
4200-b
OC-12
4010
4200-a
4020
OC-3
Time Driven Switch or Time Driven Priority Switch
Low_ capacity long time frames

FIG. 40

FIG. 41


Time frame - TF2
X bits of ch 1
Channel 1
X bits of ch 2
Channel 2
X bits of ch 3
Channel 3
X bits of ch 4
Channel 4
Low_capacity channels
CTR - 002
4280
Grooming Controller
4220
Grooming System
4200
c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec
(A)
Time frame-TF1
X bits of ch 4
X bits of ch 3
X bits of ch 2
X bits of ch 1
4125
4120
4110
High_capacity channel
X bits of ch 4
X bits of ch 3
X bits of ch 2
X bits of ch 1
4135
4137
4133
4130
Time frame-TF3
(B)

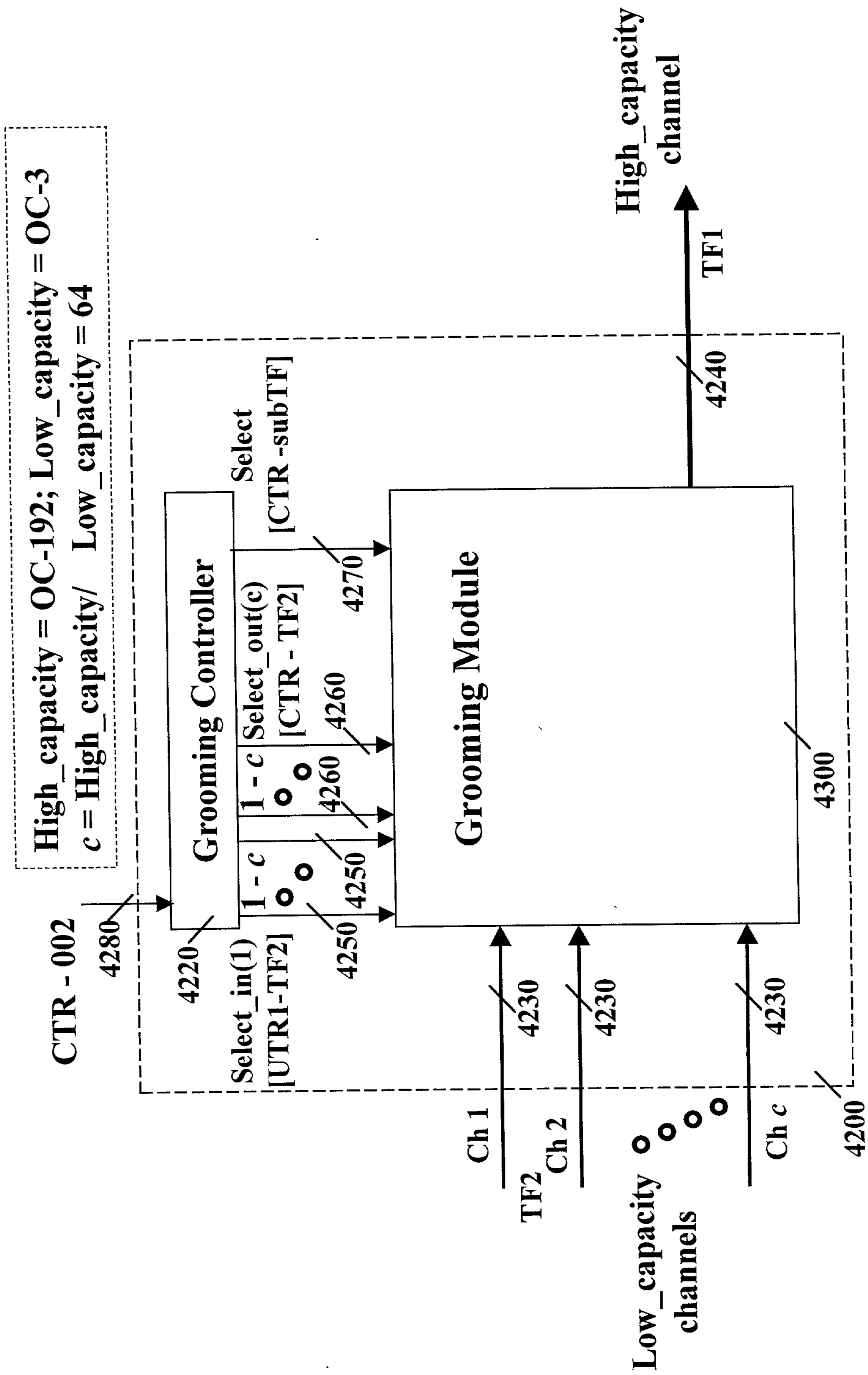

High_capacity = OC-192; Low_capacity = OC-3
c = High_capacity/ Low_capacity = 64
CTR - 002
4280
4220
Grooming Controller
Select_in(1)
[UTR1-TF2]
1 - c
4250
4250
1 - c
4260
4260
Select_out(c)
[CTR - TF2]
4270
Select
[CTR -subTF]
Grooming Module
4300
4240
TF1
High_capacity
channel
4230
4230
4230
Ch 1
Ch 2
TF2
Ch c
Low_capacity
channels
4200

FIG. 42

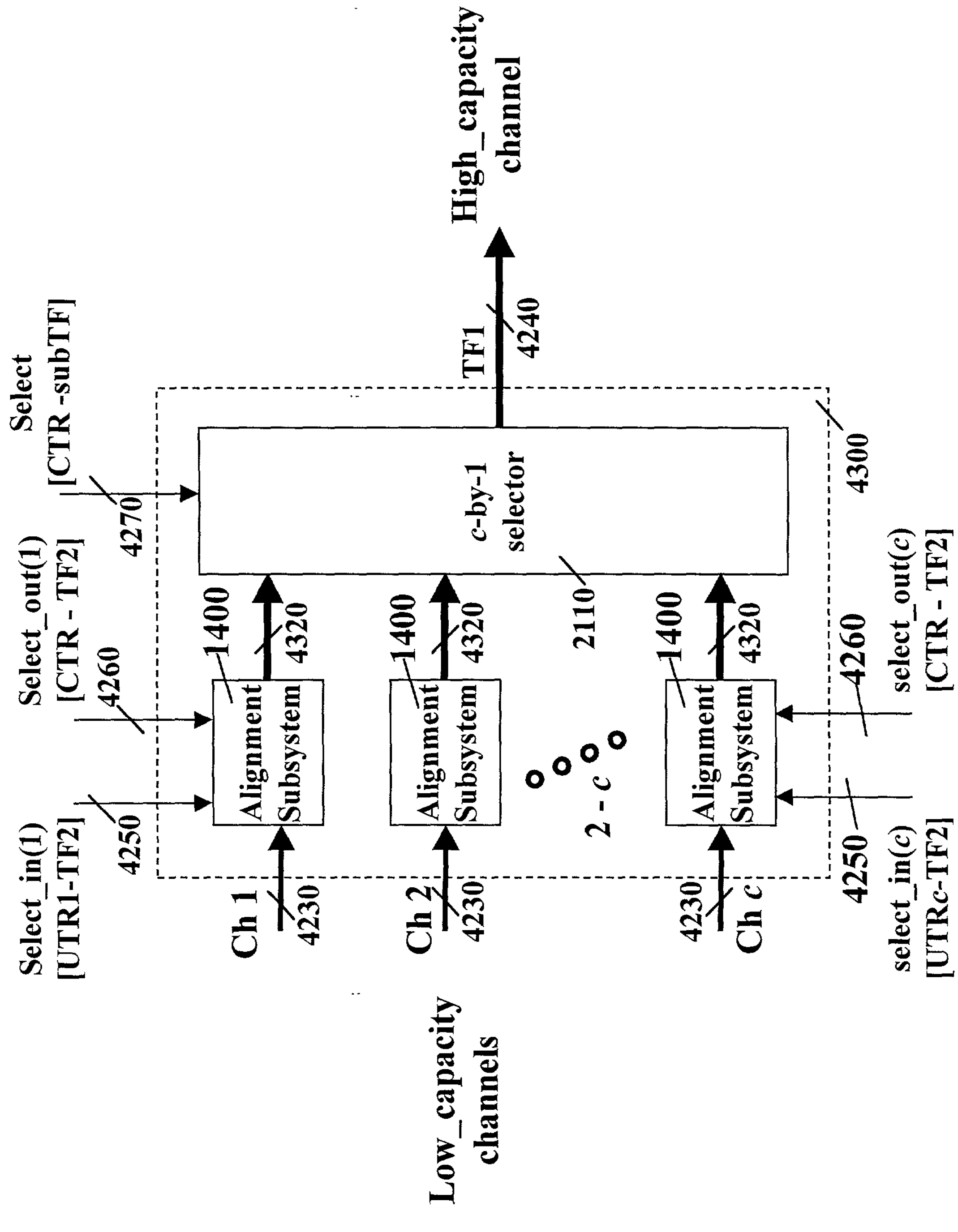

High_capacity channel
TF1
4240
Select [CTR -subTF]
4270
c-by-1 selector
2110
4300
Select_out(1) [CTR - TF2]
4260
1400
4320
Alignment Subsystem
Select_in(1) [UTR1-TF2]
4250
Ch 1
4230
Ch 2
2 - c
select_out(c) [CTR - TF2]
select_in(c) [UTRc-TF2]
Ch c
Low_capacity channels

FIG. 43

FIG. 44

- $CC1\_length \cdot TF1 = CC2\_length \cdot TF2 = CC3\_length \cdot TF2$
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the common cycles of ***TF1*** and ***TF2*** are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

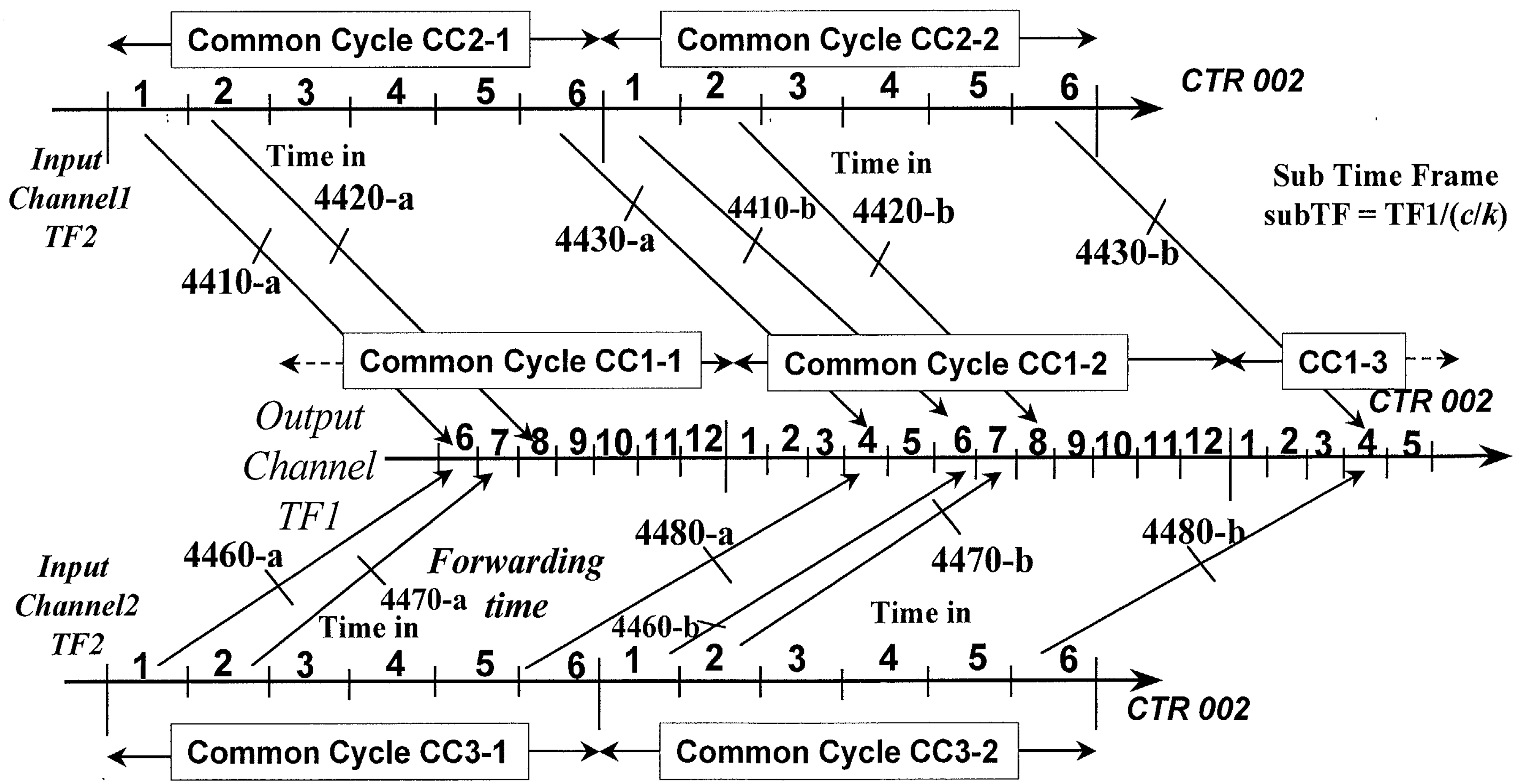


FIG. 45

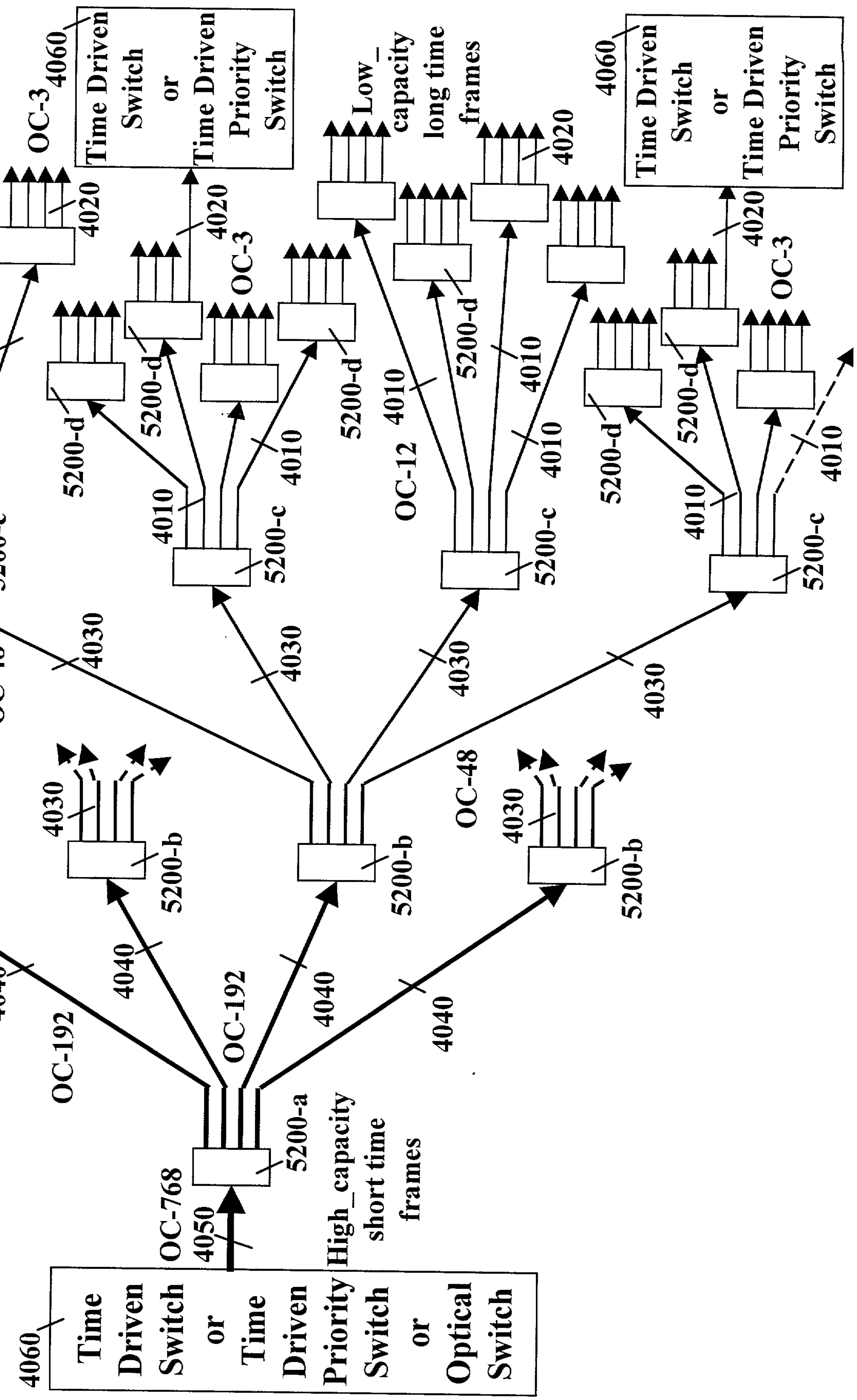
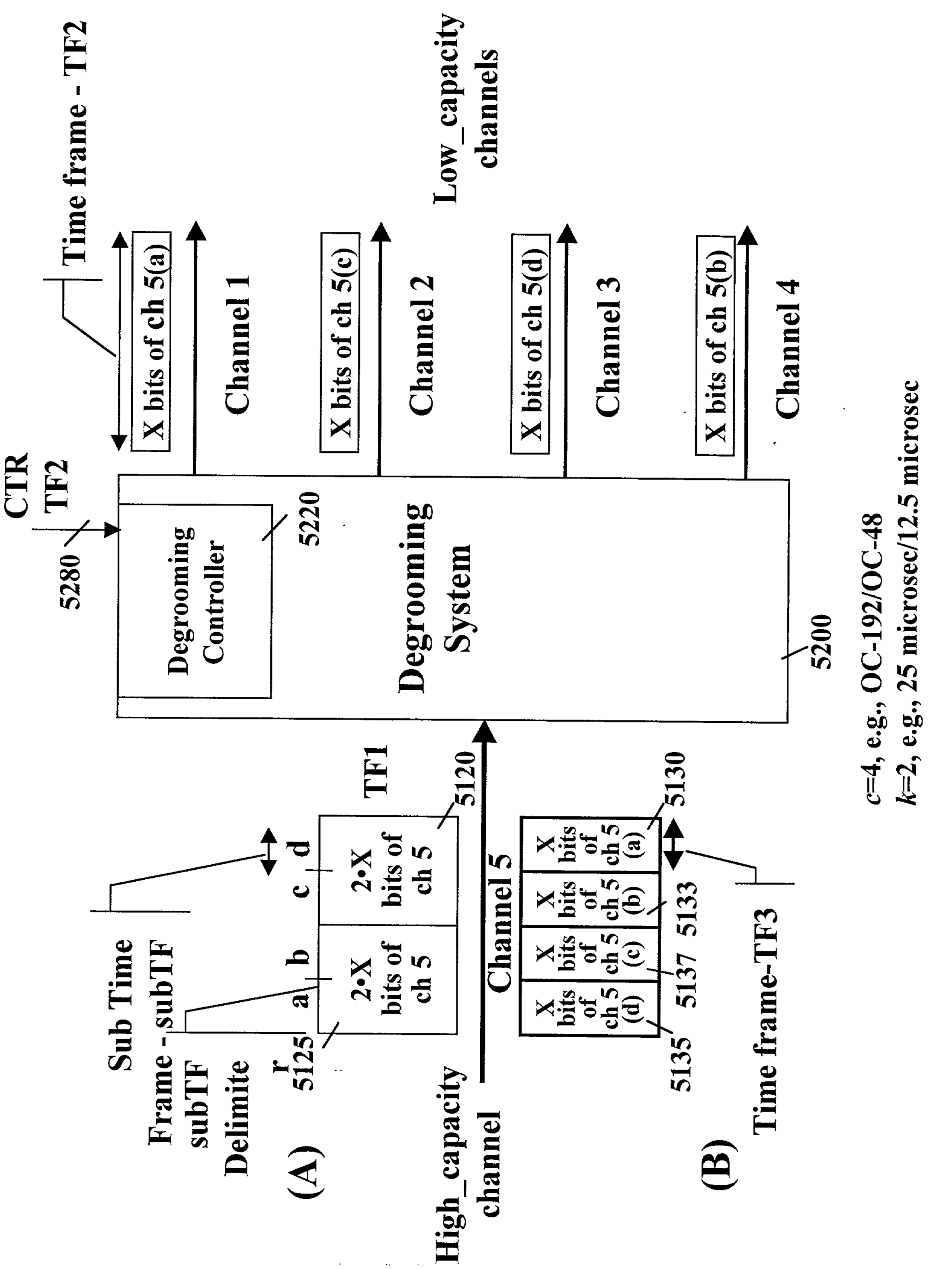

4060
Time Driven Switch or Time Driven Priority Switch or Optical Switch
4050
OC-768
High_capacity short time frames
5200-a
4040
OC-192
5200-b
4030
OC-48
5200-c
4010
OC-12
5200-d
4020
OC-3
Low_capacity long time frames
Time Driven Switch or Time Driven Priority Switch

FIG. 46


(A)
Sub Time Frame - subTF
subTF Delimiter
5125
a
b
c
d
2•X bits of ch 5
2•X bits of ch 5
5120
TF1
High_capacity channel
Channel 5
(B)
X bits of ch 5 (d)
X bits of ch 5 (c)
X bits of ch 5 (b)
X bits of ch 5 (a)
5135
5137
5133
5130
Time frame-TF3
CTR TF2
5280
Degrooming Controller
5220
Degrooming System
5200
X bits of ch 5(a)
Time frame - TF2
Channel 1
X bits of ch 5(c)
Channel 2
X bits of ch 5(d)
Channel 3
X bits of ch 5(b)
Channel 4
Low_capacity channels
c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec

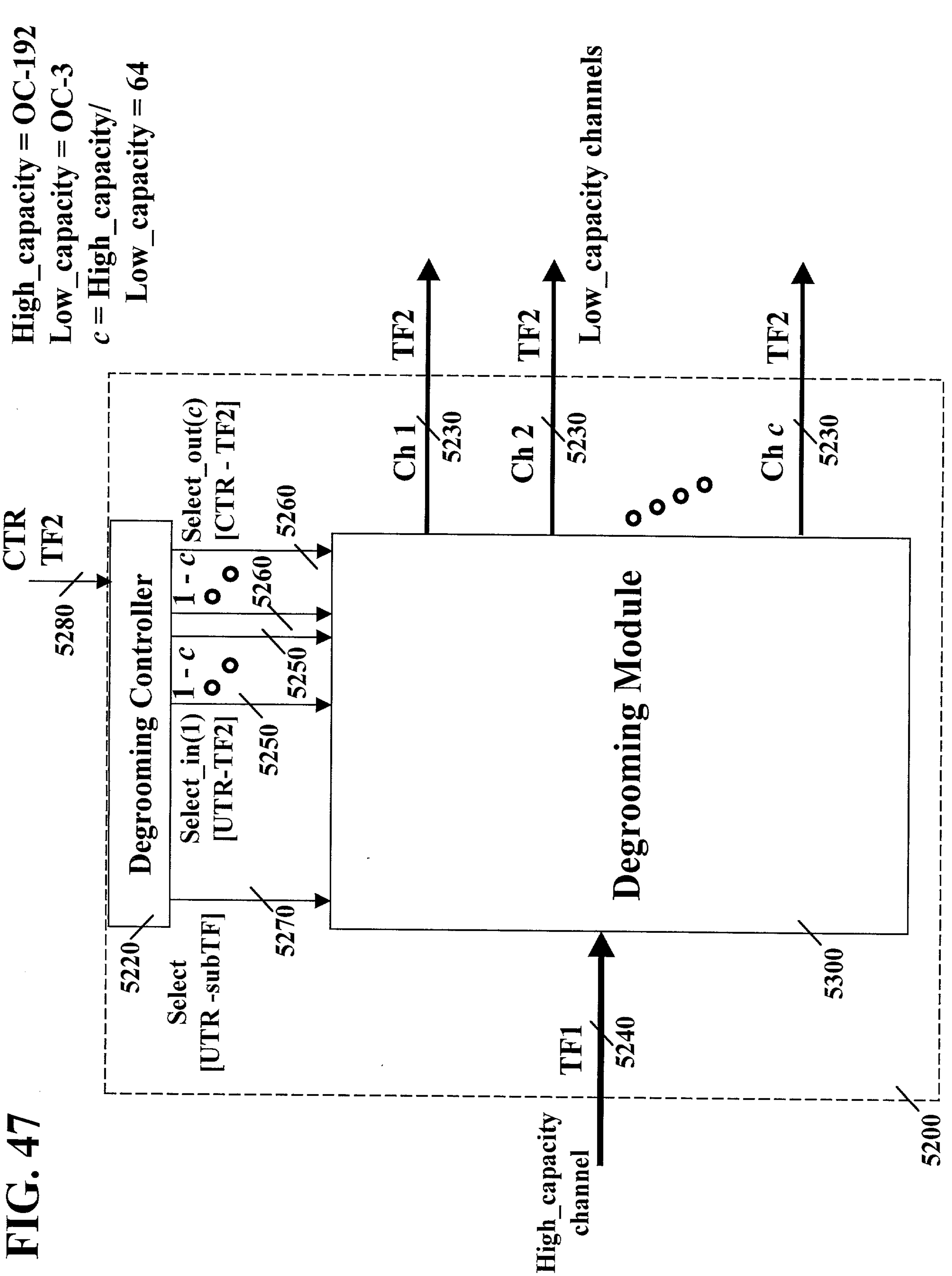
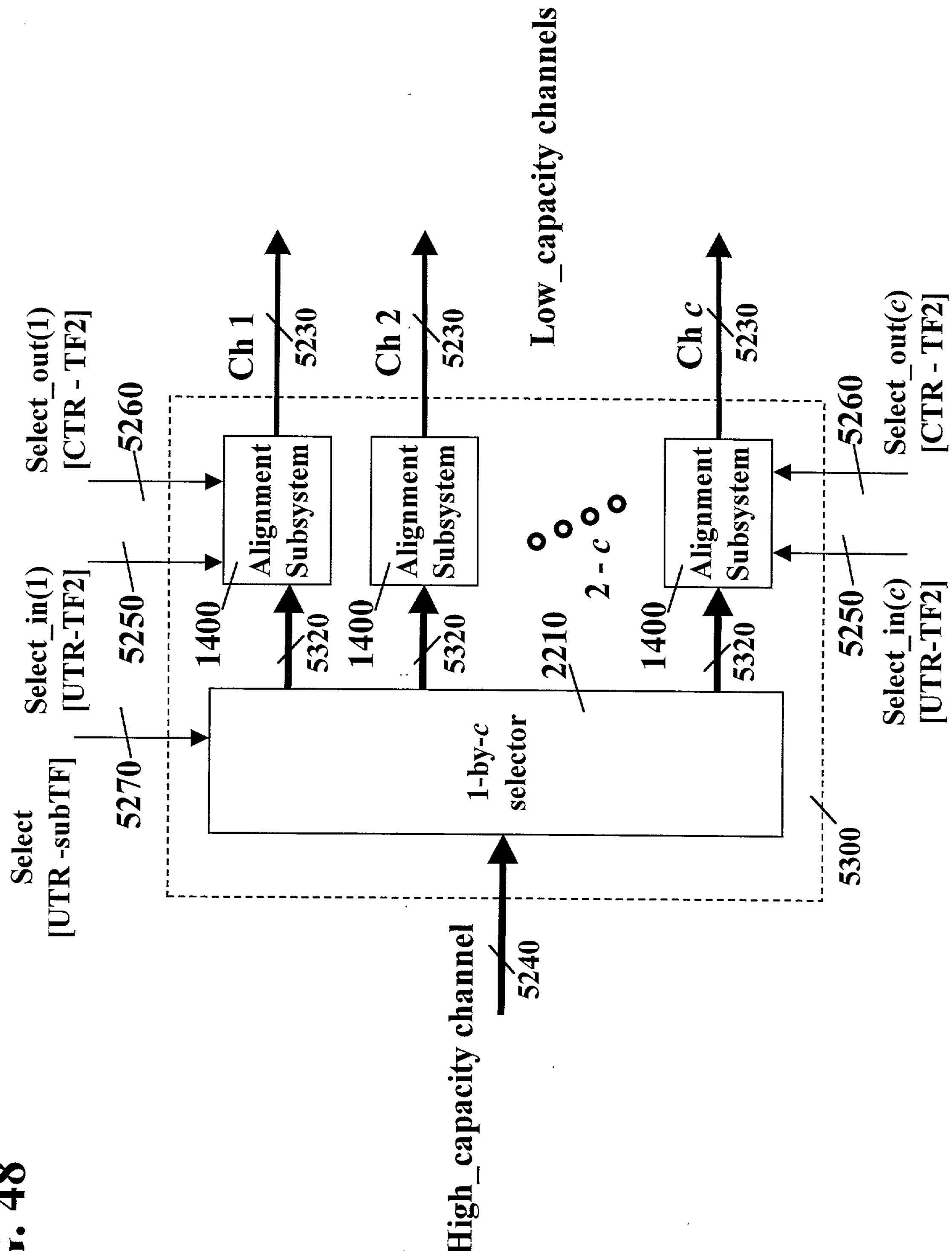

High_capacity = OC-192
Low_capacity = OC-3
c = High_capacity/
Low_capacity = 64
CTR
TF2
5280
Degrooming Controller
5220
Select
[UTR -subTF]
5270
Select_in(1)
[UTR-TF2]
1 - c
5250
5250
1 - c
5260
Select_out(c)
[CTR - TF2]
5260
Degrooming Module
5300
TF1
5240
High_capacity
channel
Ch 1
5230
TF2
Ch 2
5230
TF2
Ch c
5230
TF2
Low_capacity channels
5200

FIG. 47

FIG. 48


Low_capacity channels
High_capacity channel
Select
[UTR -subTF]
Select_in(1)
[UTR-TF2]
Select_out(1)
[CTR - TF2]
Select_in(c)
[UTR-TF2]
Select_out(c)
[CTR - TF2]
Ch 1
Ch 2
Ch c
Alignment
Subsystem
1-by-c
selector
2 - c
5230
5240
5250
5260
5270
5300
5320
1400
2210

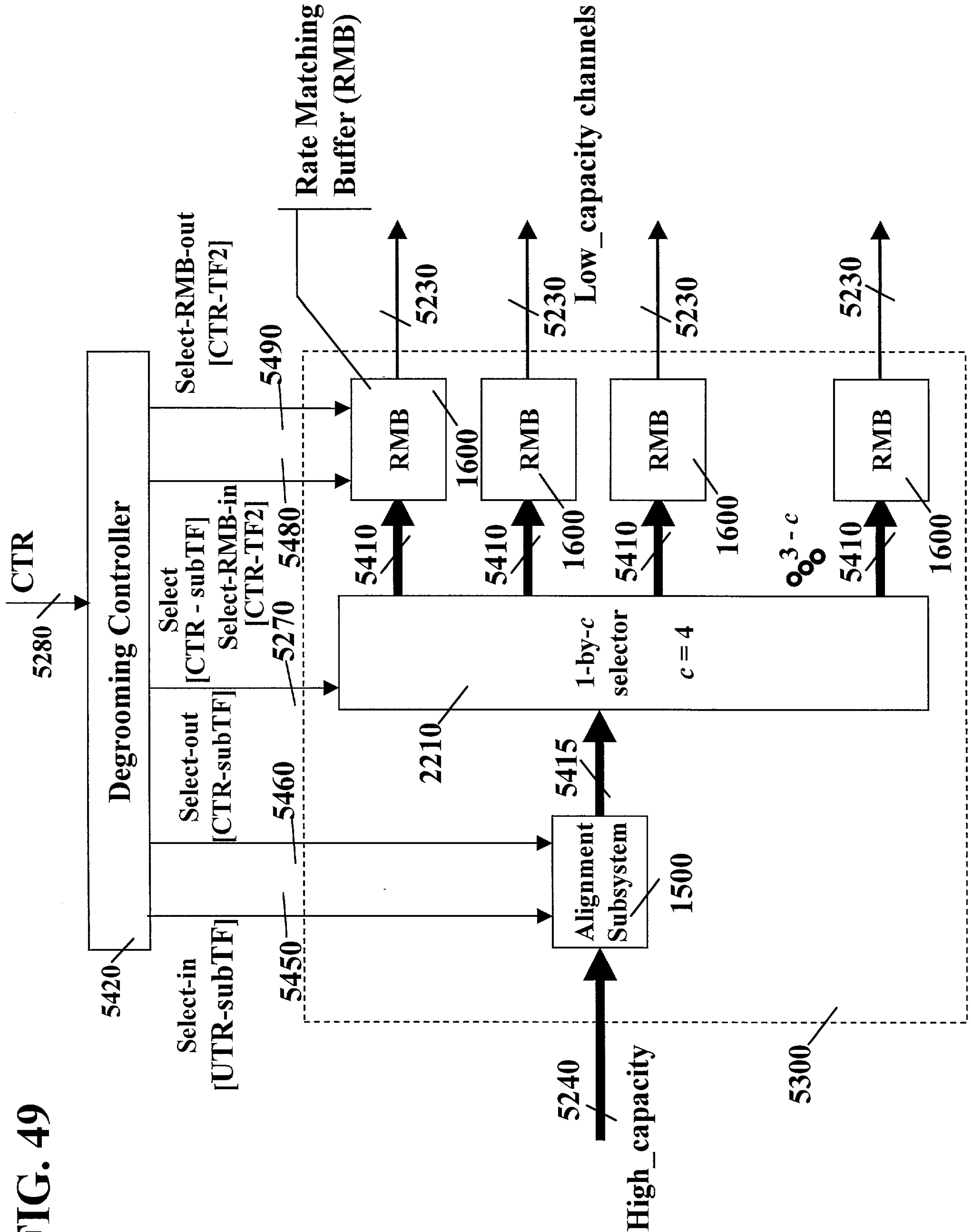

CTR
5280
Degrooming Controller
5420
Select-in
[UTR-subTF]
5450
Select-out
[CTR-subTF]
5460
Select
[CTR - subTF]
5270
Select-RMB-in
[CTR-TF2]
5480
Select-RMB-out
[CTR-TF2]
5490
Rate Matching
Buffer (RMB)
RMB
1600
5230
Low_capacity channels
5410
1-by-c
selector
c = 4
2210
3 - c
5415
Alignment
Subsystem
1500
5240
High_capacity
5300

FIG. 49

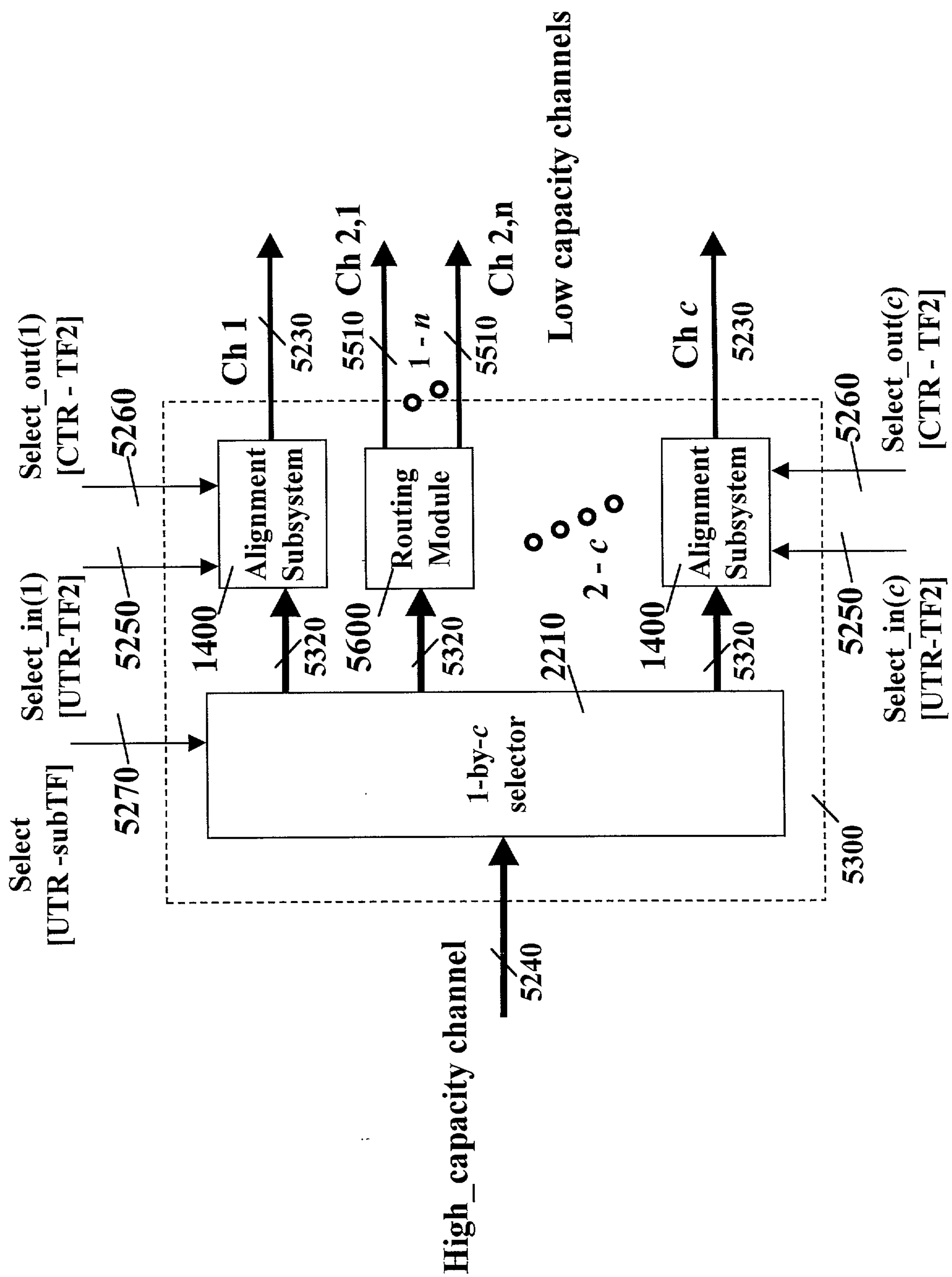

High_capacity channel
5240
Select
[UTR -subTF]
5270
Select_in(1)
[UTR-TF2]
5250
Select_out(1)
[CTR - TF2]
5260
1-by-c selector
2210
5300
5320
1400
Alignment Subsystem
5600
Routing Module
2 - c
Ch 1
5230
5510
Ch 2,1
1 - n
Ch 2,n
Low capacity channels
Ch c
Select_in(c)
[UTR-TF2]
Select_out(c)
[CTR - TF2]

FIG. 50

FIG. 51

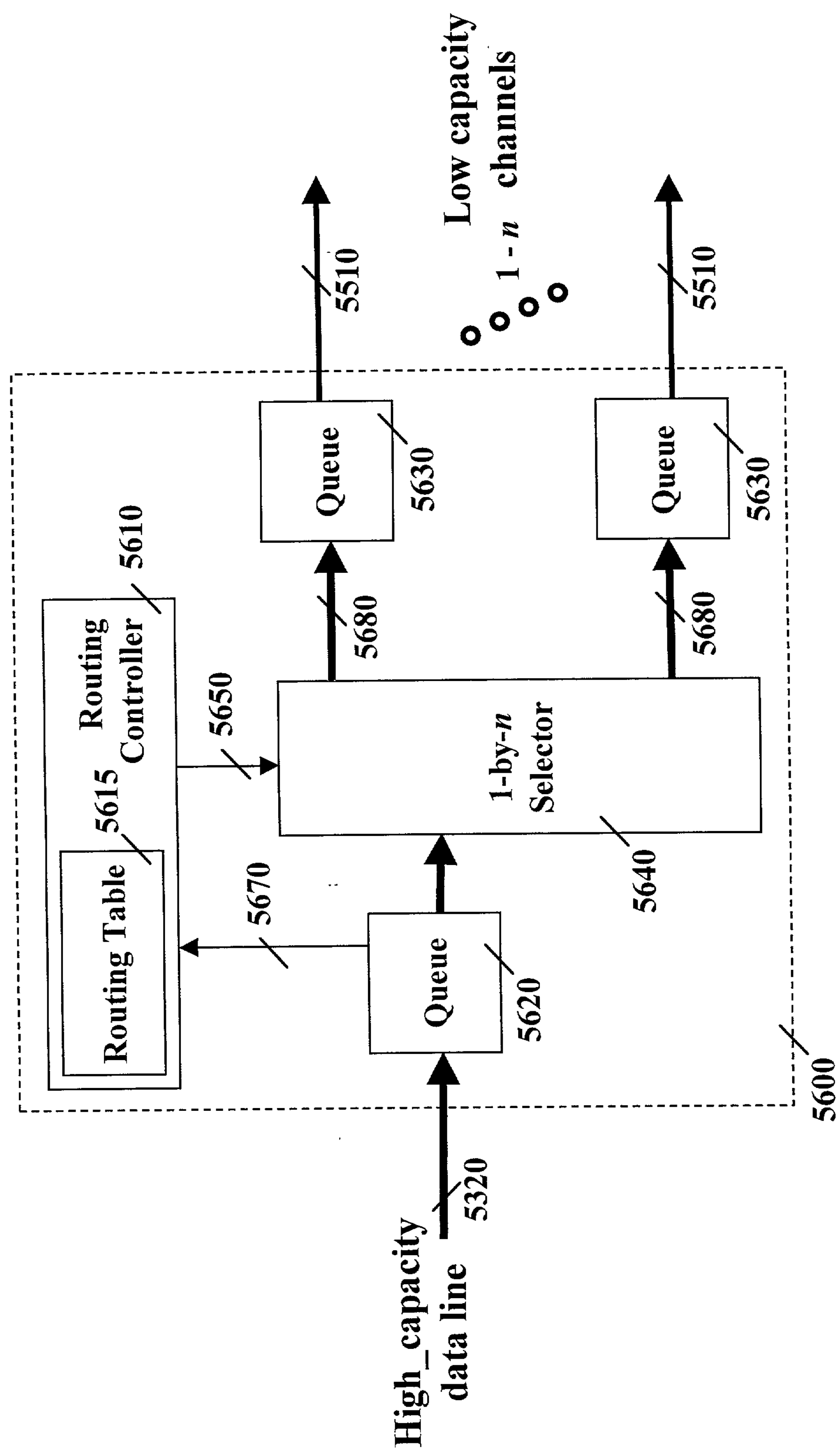

High_capacity data line
5320
Queue
5620
Routing Table
5615
Routing Controller
5610
5670
5650
1-by-n Selector
5640
5680
5680
Queue
5630
Queue
5630
5510
5510
1 - n
Low capacity channels
5600

FIG. 52

- $CC1\_length \cdot TF1 = CC2\_length \cdot TF2 = CC3\_length \cdot TF2$
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the common cycles of *TF1* and *TF2* are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

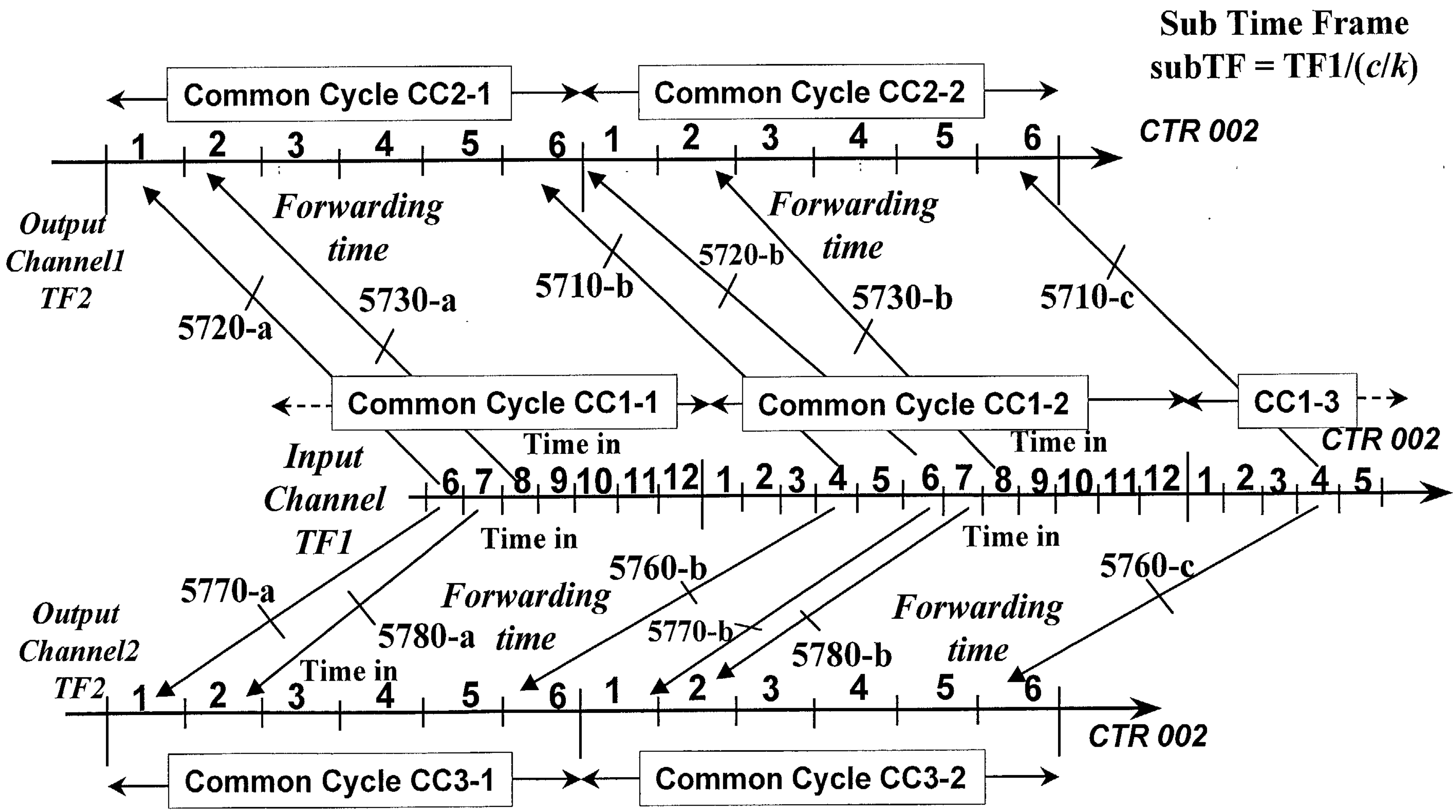


FIG. 53

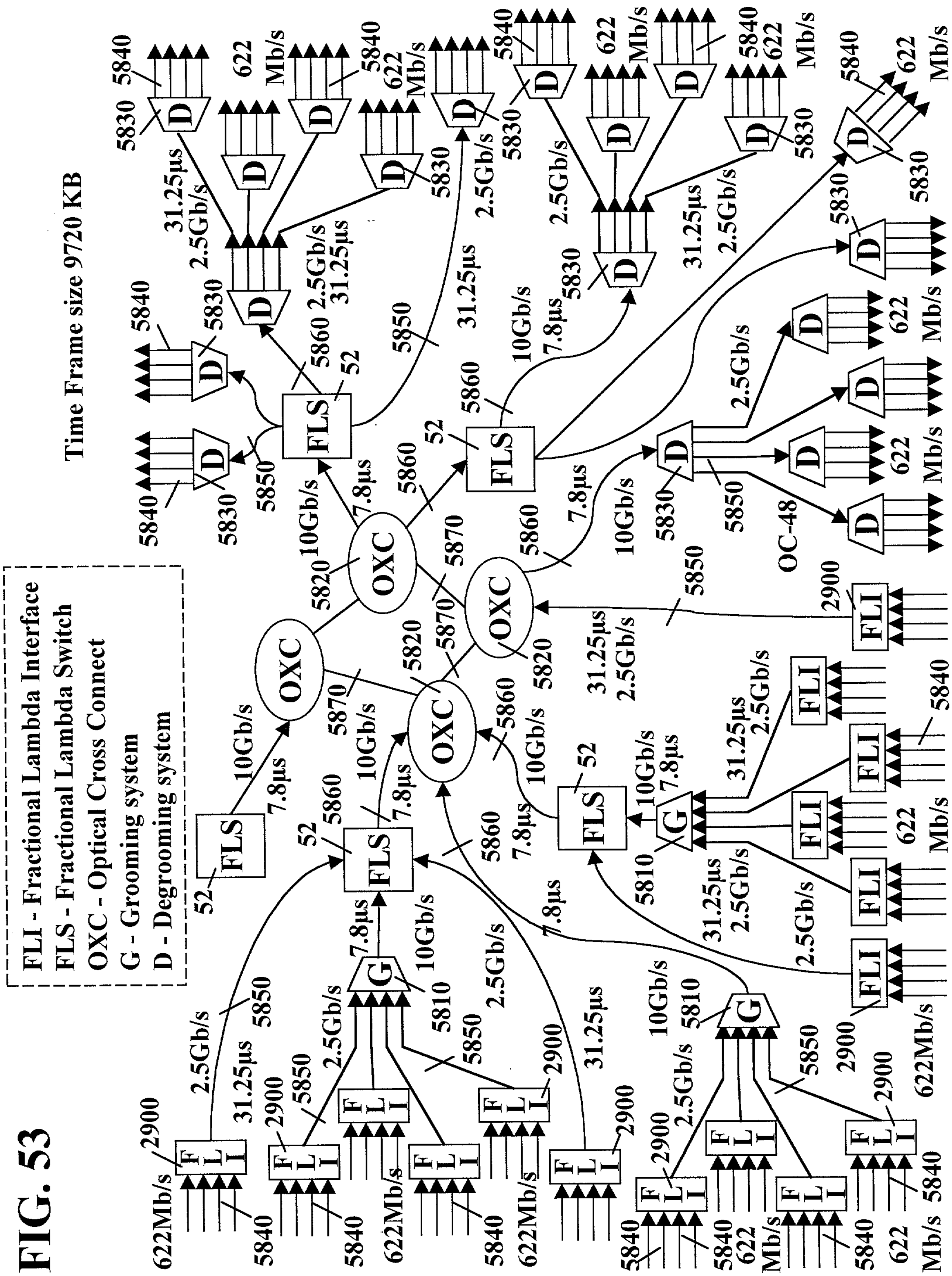

Time Frame size 9720 KB
FLI - Fractional Lambda Interface
FLS - Fractional Lambda Switch
OXC - Optical Cross Connect
G - Grooming system
D - Degrooming system
FLI
FLS
OXC
G
D
52
2900
5810
5820
5830
5840
5850
5860
5870
622Mb/s
2.5Gb/s
10Gb/s
31.25μs
7.8μs
OC-48

FIG. 54

12 STS-1s per time frame

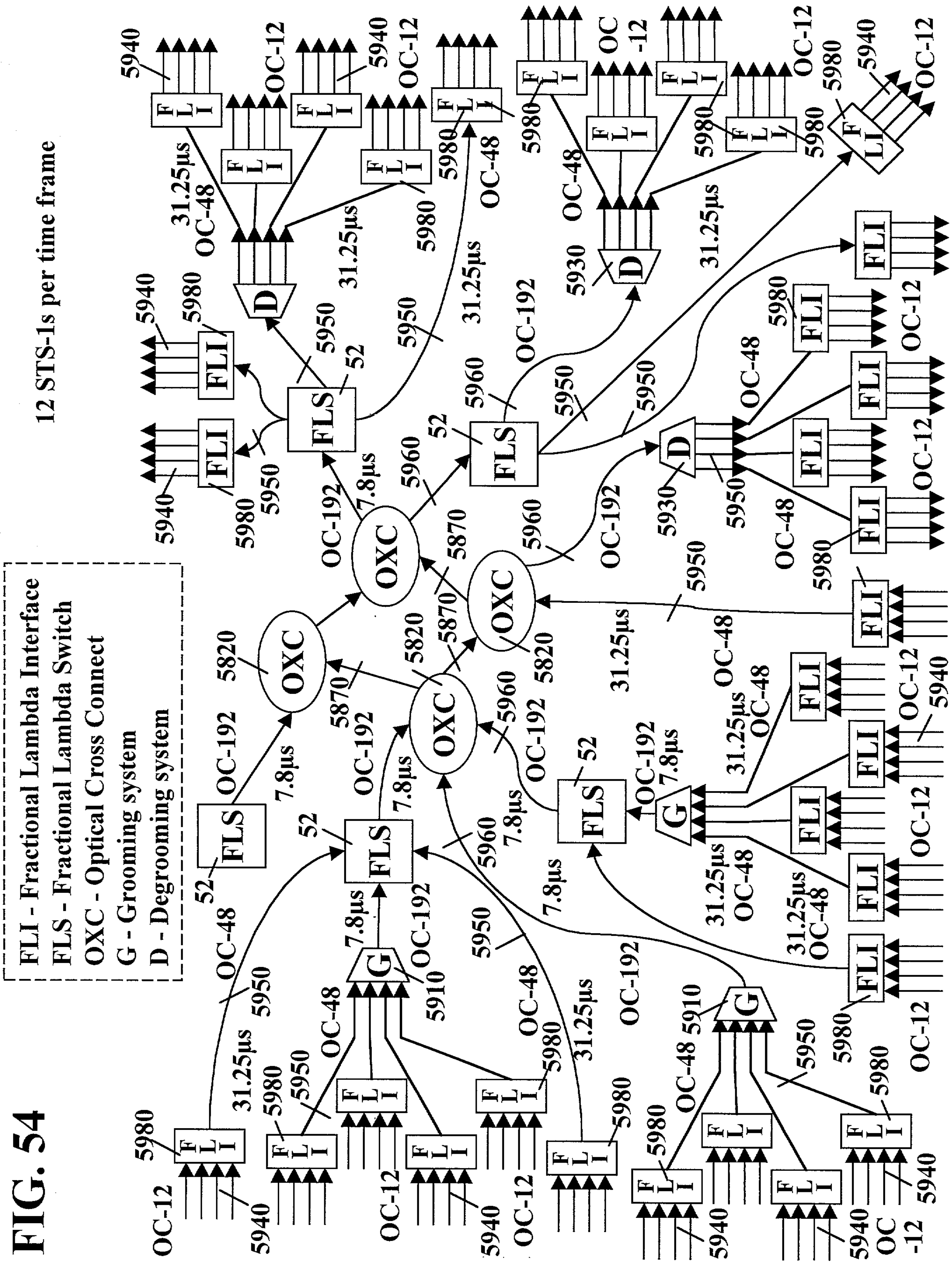
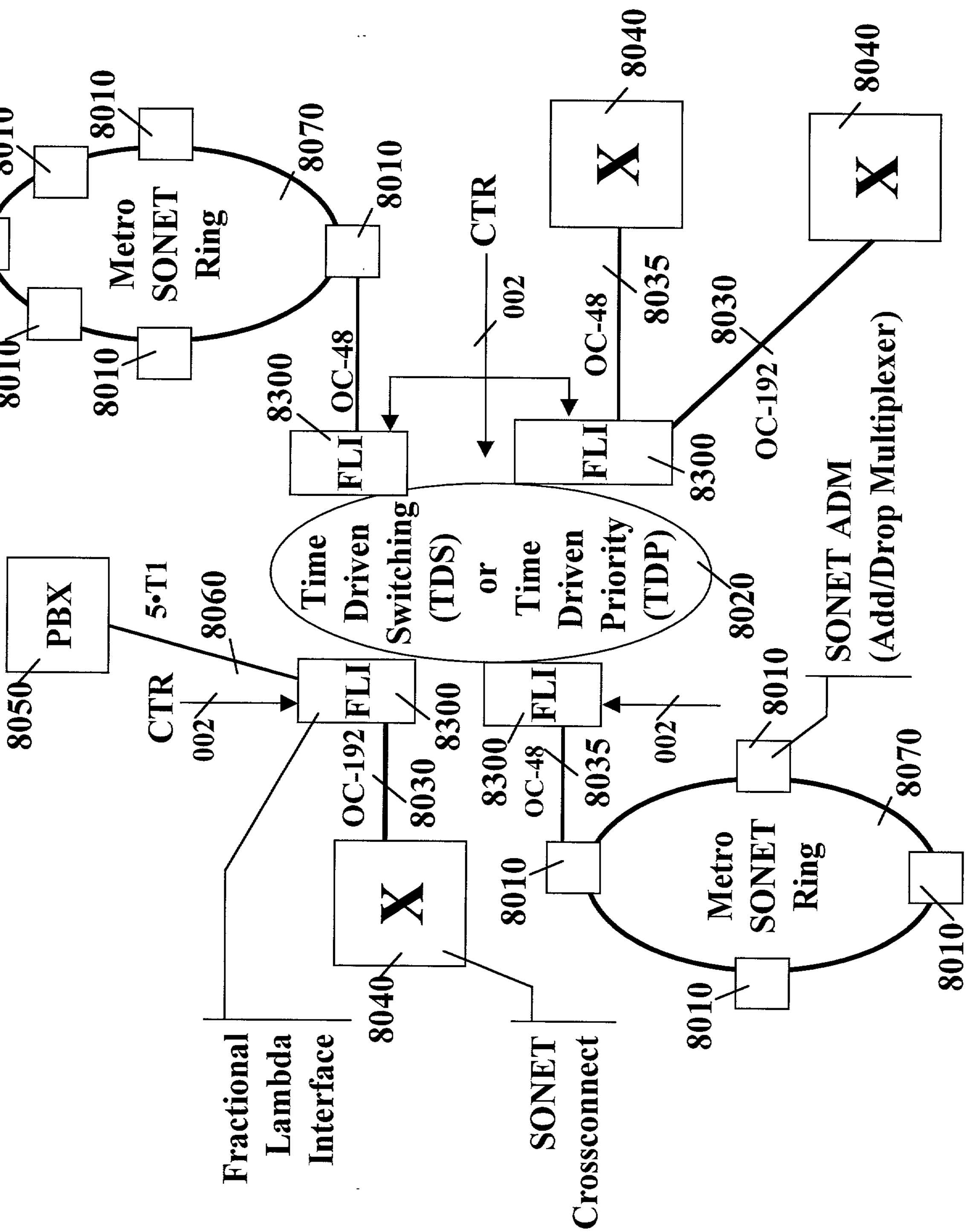


FIG. 55


Metro SONET Ring
8070
8010
OC-48
8300
FLI
CTR
002
8040
X
8035
8030
OC-192
Time Driven Switching (TDS) or Time Driven Priority (TDP)
8020
PBX
8050
5•T1
8060
SONET ADM (Add/Drop Multiplexer)
Fractional Lambda Interface
SONET Crossconnect

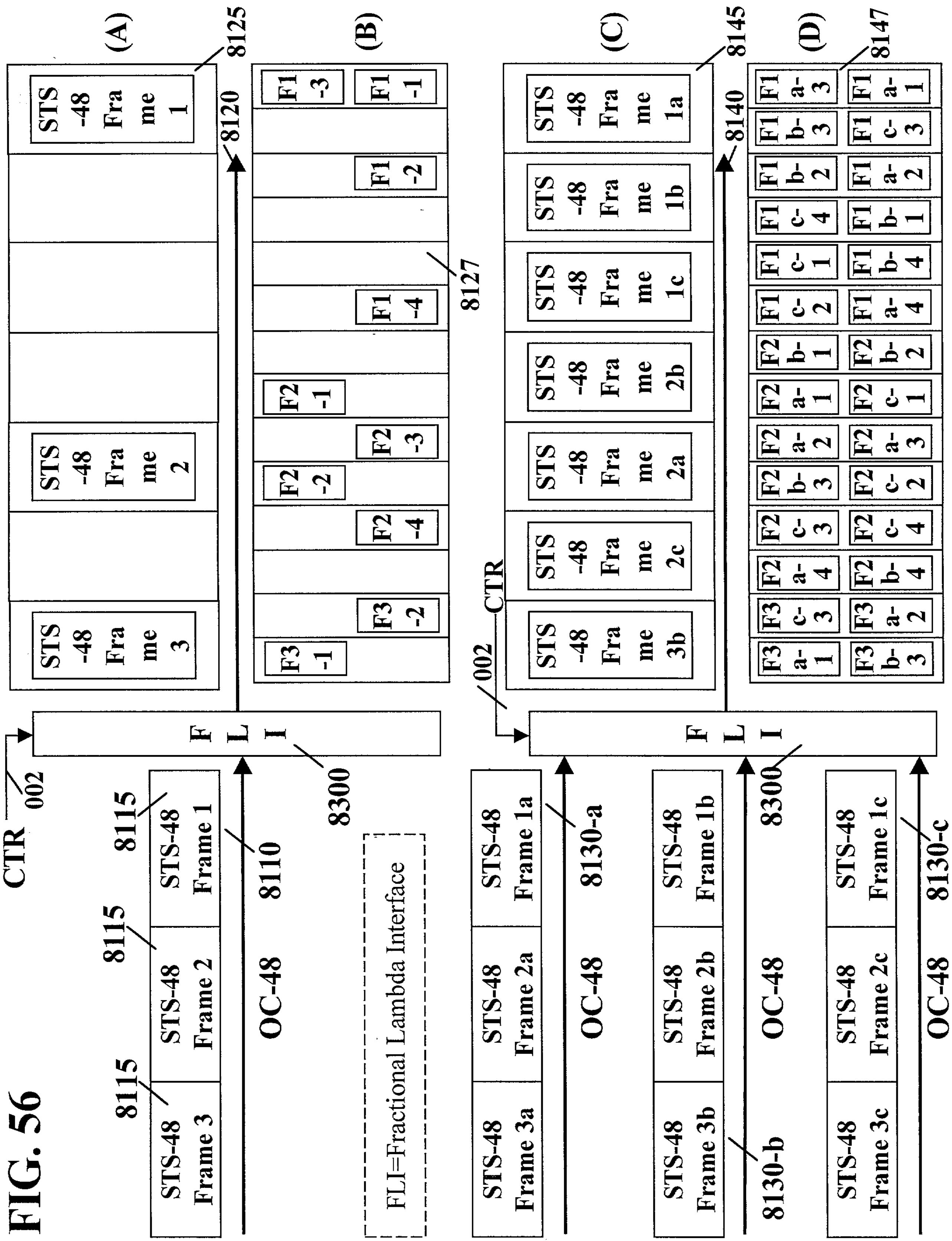

CTR
002
8115
STS-48 Frame 1
STS-48 Frame 2
STS-48 Frame 3
8110
OC-48
FLI
8300
FLI=Fractional Lambda Interface
8120
8125
(A)
STS-48 Frame 1
STS-48 Frame 2
STS-48 Frame 3
(B)
8127
F1-1
F1-2
F1-3
F1-4
F2-1
F2-2
F2-3
F2-4
F3-1
F3-2
STS-48 Frame 1a
STS-48 Frame 2a
STS-48 Frame 3a
8130-a
STS-48 Frame 1b
STS-48 Frame 2b
STS-48 Frame 3b
8130-b
STS-48 Frame 1c
STS-48 Frame 2c
STS-48 Frame 3c
8130-c
8140
8145
(C)
STS-48 Frame 1a
STS-48 Frame 1b
STS-48 Frame 1c
STS-48 Frame 2b
STS-48 Frame 2a
STS-48 Frame 2c
STS-48 Frame 3b
(D)
8147
F1 a-3
F1 b-3
F1 b-2
F1 c-4
F1 c-1
F1 c-2
F2 b-1
F2 a-1
F2 a-2
F2 b-3
F2 c-3
F2 a-4
F3 c-3
F3 a-1
F1 a-1
F1 c-3
F1 a-2
F1 b-1
F1 b-4
F1 a-4
F2 b-2
F2 c-1
F2 a-3
F2 c-2
F2 c-4
F2 b-4
F3 a-2
F3 b-3

FIG. 56

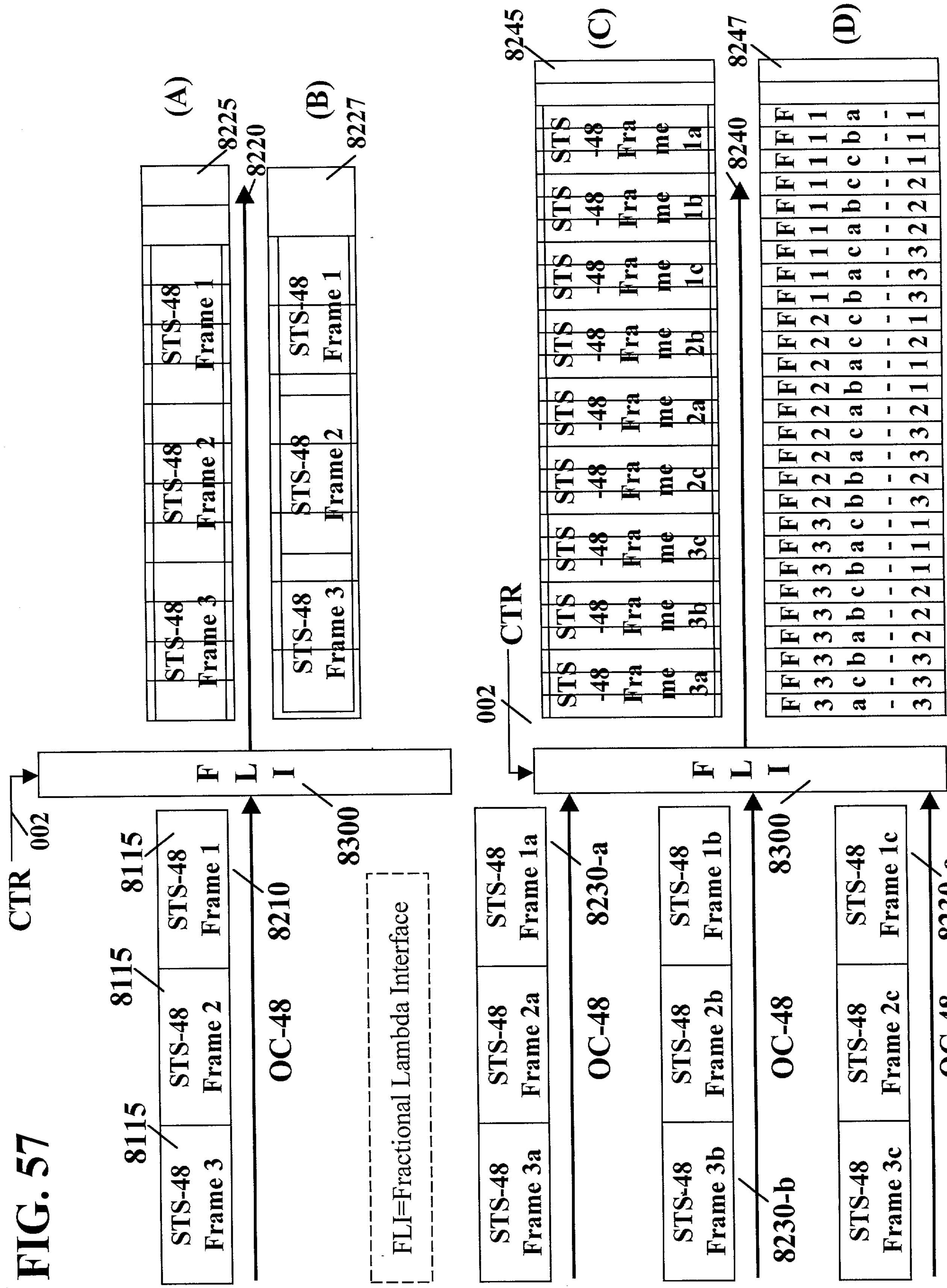

CTR
002
8115
STS-48 Frame 3
STS-48 Frame 2
STS-48 Frame 1
OC-48
8210
FLI
8300
8220
8225
(A)
8227
(B)
FLI=Fractional Lambda Interface
STS-48 Frame 3a
STS-48 Frame 2a
STS-48 Frame 1a
8230-a
STS-48 Frame 3b
STS-48 Frame 2b
STS-48 Frame 1b
8230-b
STS-48 Frame 3c
STS-48 Frame 2c
STS-48 Frame 1c
8230-c
8240
8245
(C)
STS-48 Frame 3a
STS-48 Frame 3b
STS-48 Frame 3c
STS-48 Frame 2c
STS-48 Frame 2a
STS-48 Frame 2b
STS-48 Frame 1c
STS-48 Frame 1b
STS-48 Frame 1a
8247
(D)

FIG. 57

FIG. 58

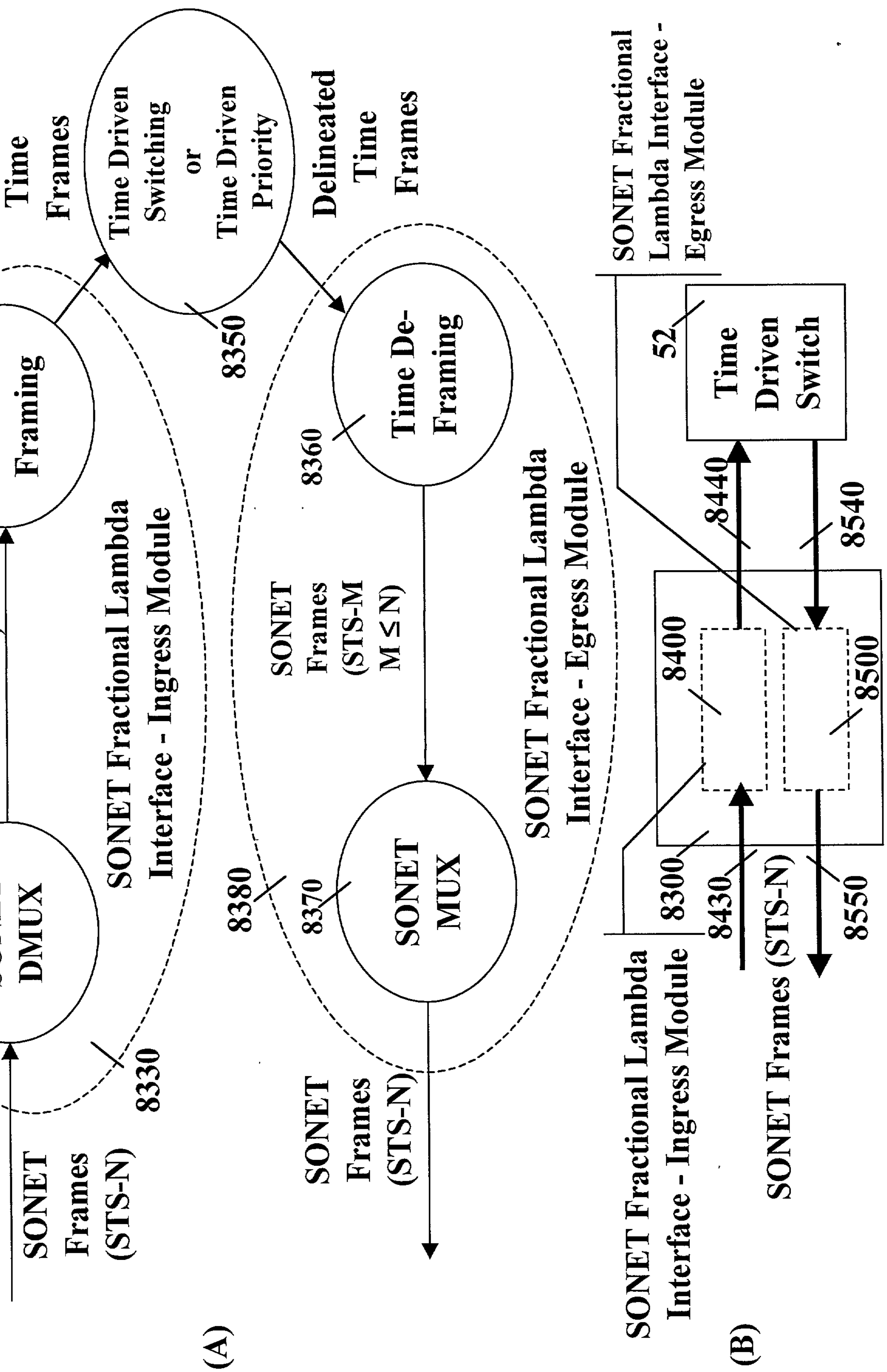
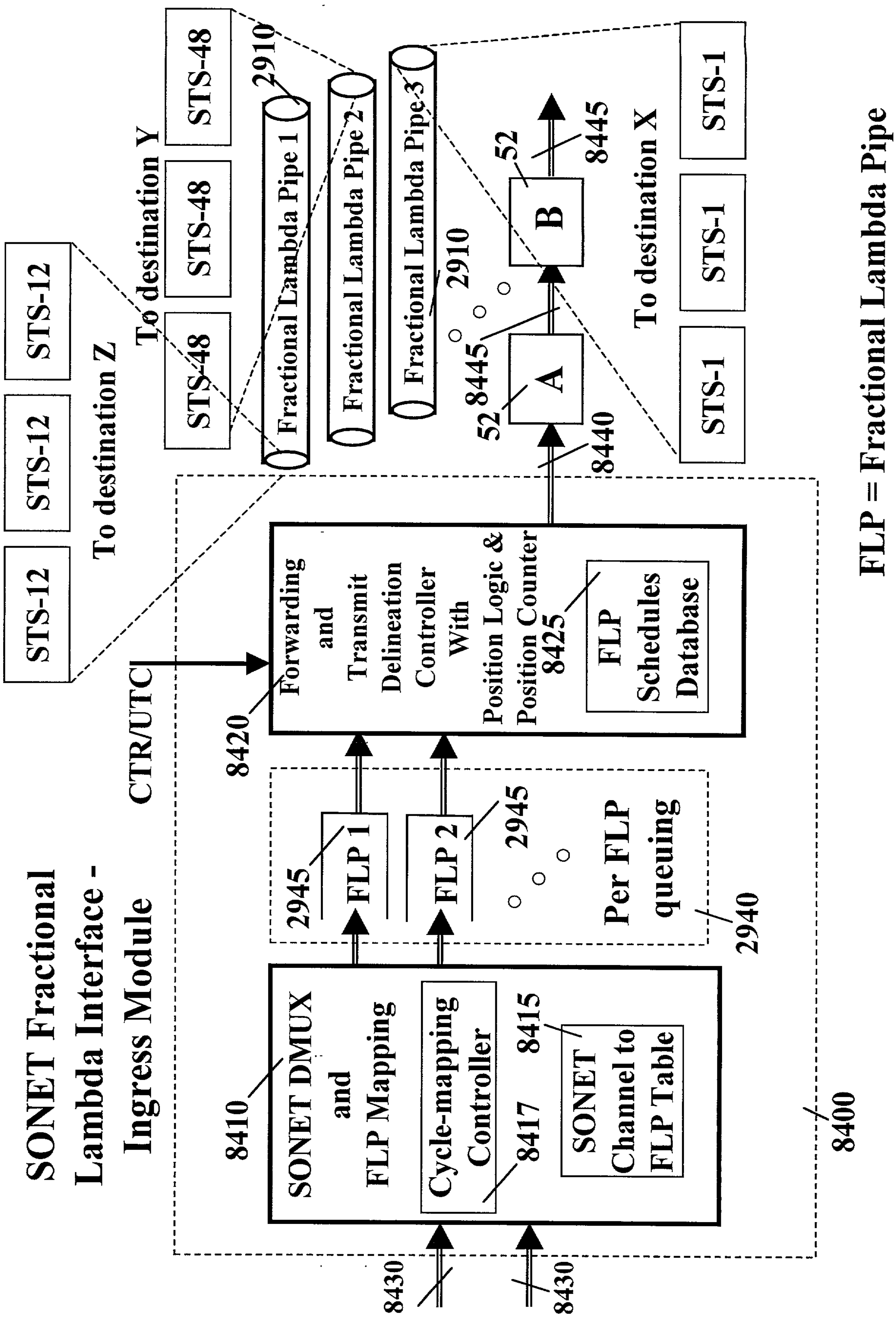

(A)
SONET Frames (STS-N)
SONET DMUX
8310
8330
SONET Frames (STS-M M ≤ N)
Time Framing
8320
SONET Fractional Lambda Interface - Ingress Module
Delineated Time Frames
Time Driven Switching or Time Driven Priority
8350
Delineated Time Frames
Time De-Framing
8360
SONET Frames (STS-M M ≤ N)
SONET MUX
8370
8380
SONET Fractional Lambda Interface - Egress Module
SONET Frames (STS-N)
(B)
SONET Fractional Lambda Interface - Ingress Module
SONET Frames (STS-N)
8300
8430
8550
8400
8500
8440
8540
52
Time Driven Switch
SONET Fractional Lambda Interface - Egress Module

FIG. 59

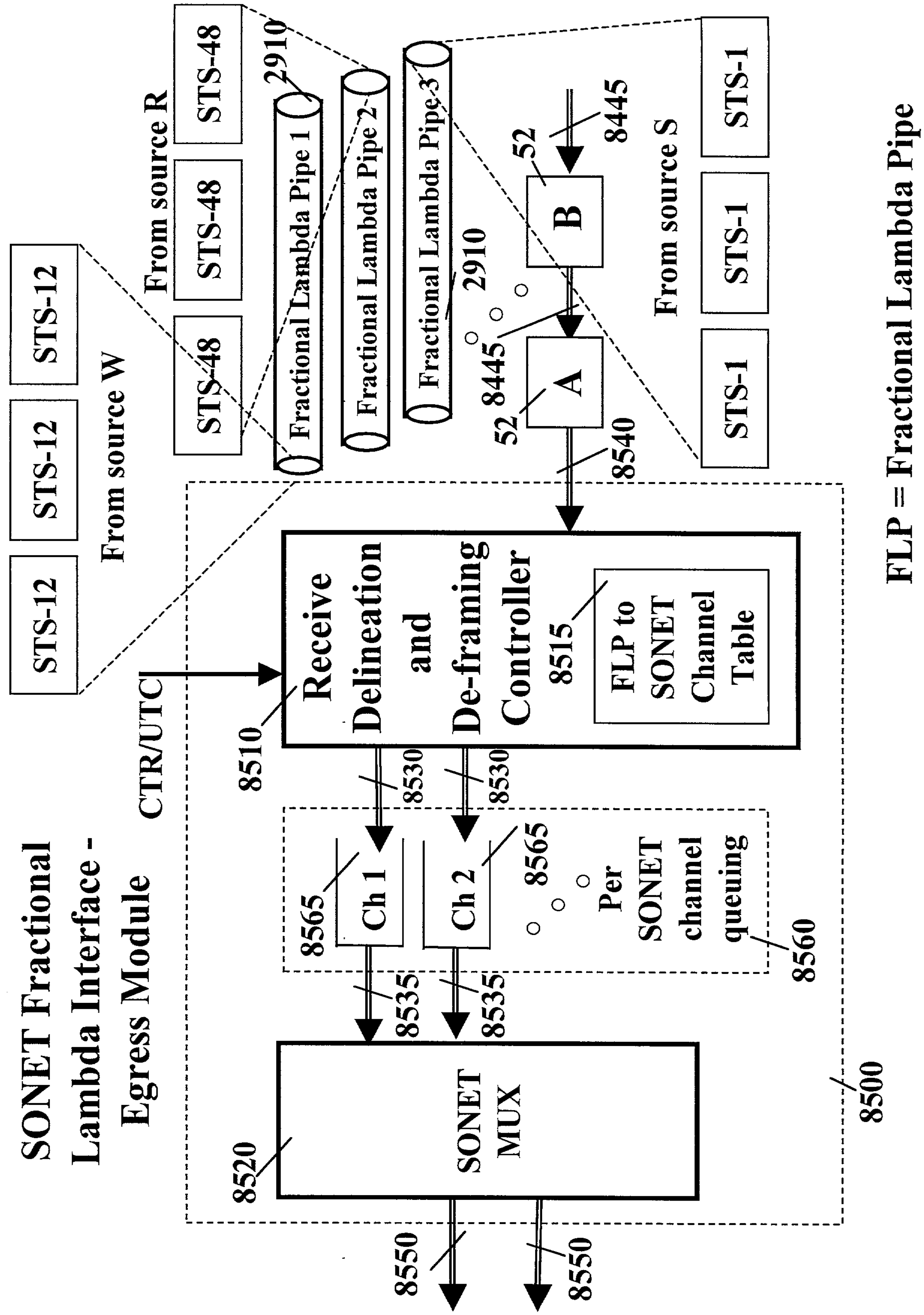
SONET Fractional Lambda Interface - Ingress Module



FLP = Fractional Lambda Pipe

FIG. 60

SONET Fractional Lambda Interface - Egress Module



FLP = Fractional Lambda Pipe

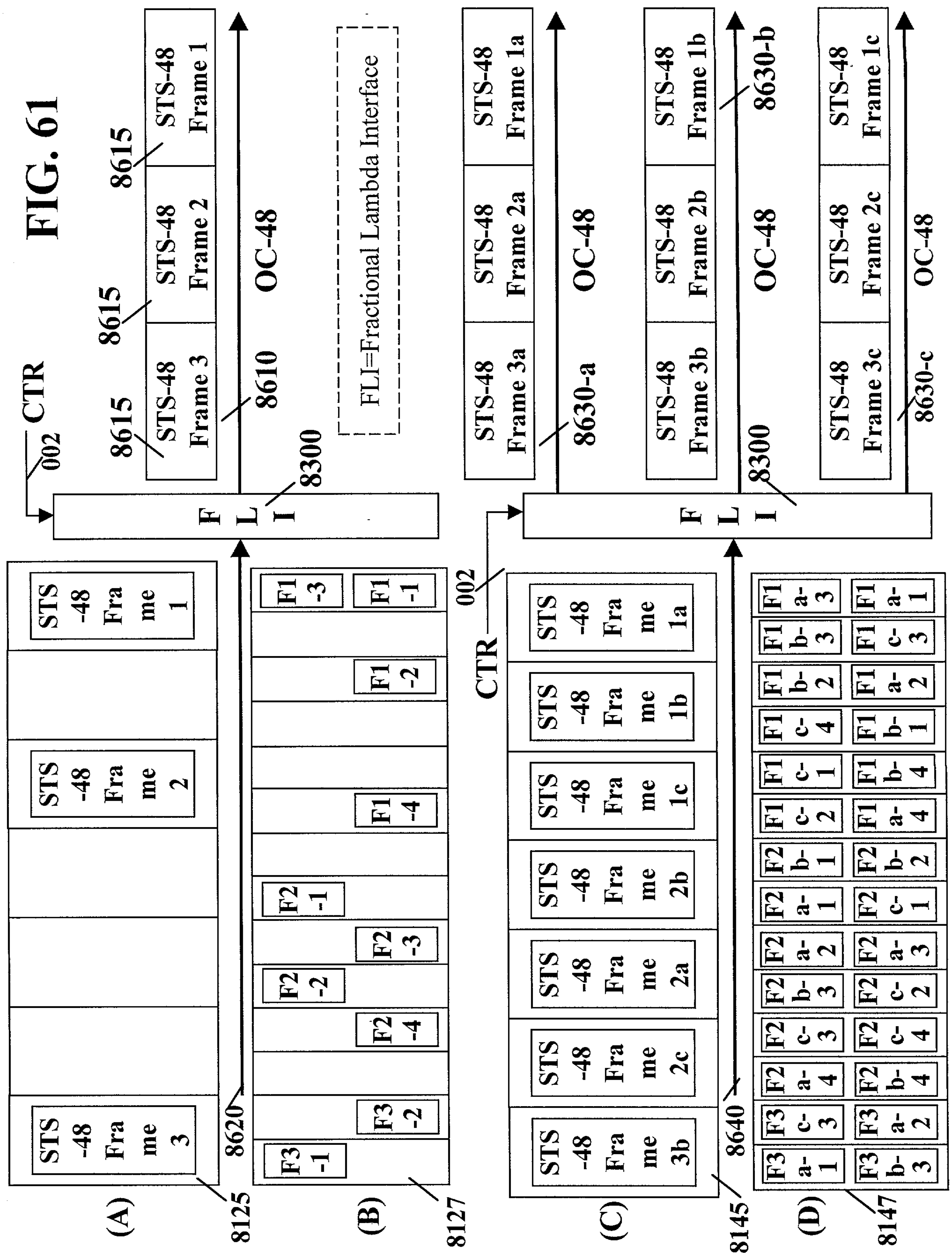
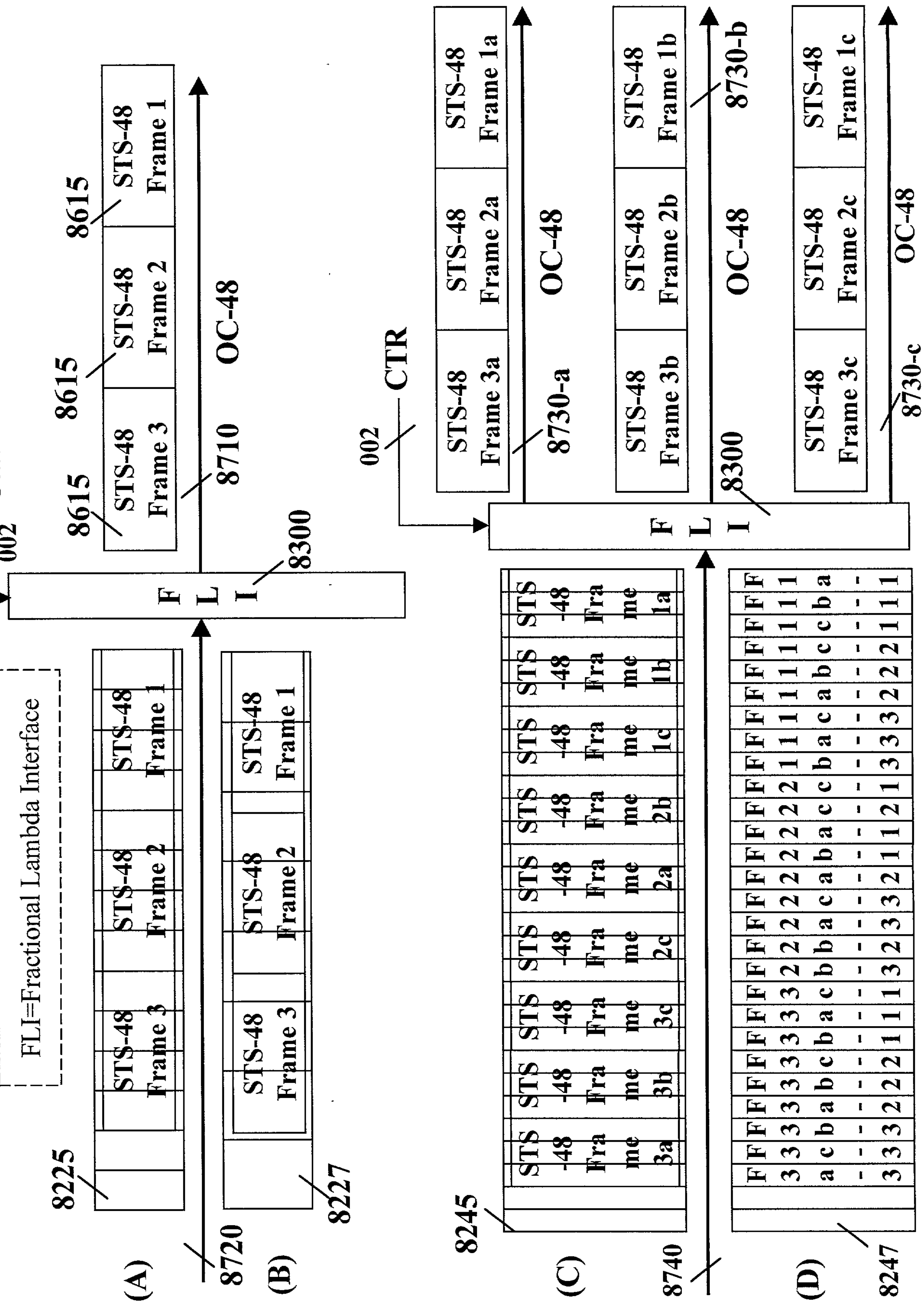

CTR
002
8615
STS-48 Frame 3
STS-48 Frame 2
STS-48 Frame 1
8610
OC-48
8300
FLI
FLI=Fractional Lambda Interface
STS-48 Frame 3a
STS-48 Frame 2a
STS-48 Frame 1a
8630-a
STS-48 Frame 3b
STS-48 Frame 2b
STS-48 Frame 1b
8630-b
STS-48 Frame 3c
STS-48 Frame 2c
STS-48 Frame 1c
8630-c
(A)
8125
STS-48 Frame 3
STS-48 Frame 2
STS-48 Frame 1
8620
(B)
8127
F3-1
F3-2
F2-4
F2-2
F2-3
F2-1
F1-4
F1-2
F1-3
F1-1
(C)
8145
STS-48 Frame 3b
STS-48 Frame 2c
STS-48 Frame 2a
STS-48 Frame 2b
STS-48 Frame 1c
STS-48 Frame 1b
STS-48 Frame 1a
8640
(D)
8147
F3 a-1
F3 c-3
F2 a-4
F2 c-3
F2 b-3
F2 a-2
F2 a-1
F2 b-1
F1 c-2
F1 c-1
F1 c-4
F1 b-2
F1 b-3
F1 a-3
F3 b-3
F3 a-2
F2 b-4
F2 c-4
F2 c-2
F2 a-3
F2 c-1
F2 b-2
F1 a-4
F1 b-4
F1 b-1
F1 a-2
F1 c-3
F1 a-1

FIG. 61

FIG. 62


FLI=Fractional Lambda Interface
(A)
(B)
(C)
(D)
8225
8227
8720
8710
8300
002
CTR
FLI
8615
STS-48 Frame 1
STS-48 Frame 2
STS-48 Frame 3
OC-48
8245
8247
8740
8730-a
8730-b
8730-c
STS-48 Frame 1a
STS-48 Frame 2a
STS-48 Frame 3a
STS-48 Frame 1b
STS-48 Frame 2b
STS-48 Frame 3b
STS-48 Frame 1c
STS-48 Frame 2c
STS-48 Frame 3c

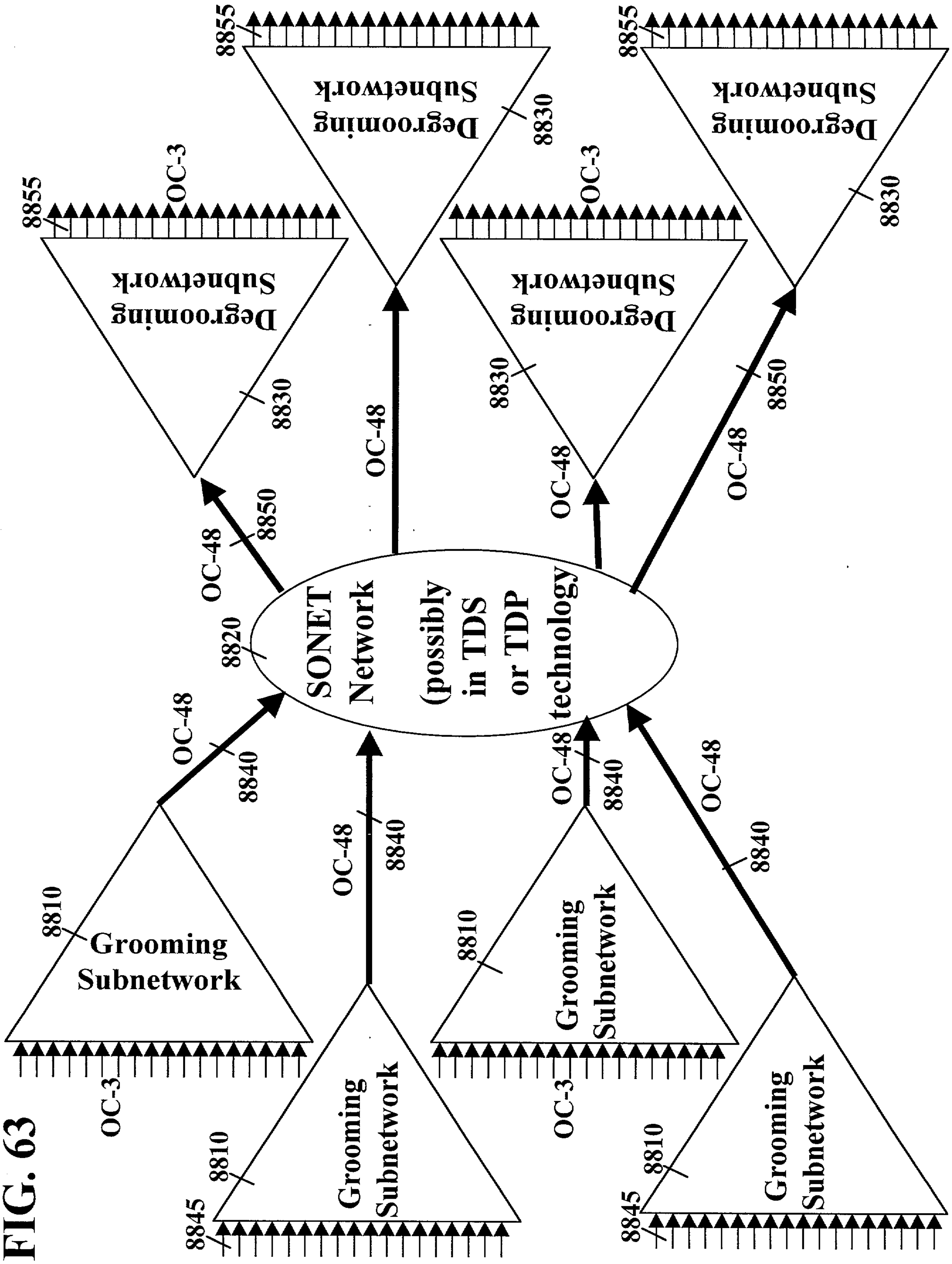

Grooming Subnetwork
8810
OC-3
8845
OC-48
8840
SONET Network (possibly in TDS or TDP technology)
8820
8850
Degrooming Subnetwork
8830
8855

FIG. 63

FIG. 64

- SONET - synchronous optical network
- Multiplexing method: byte interleaving
- Signal hierarchy: OC-N (STS-N)
  - STS-N rate: N*51.84 Mb/s
  - Frame format: 9 rows by 90*N columns
    - capacity: N*810 bytes in 125 microsecond.
    - overhead: N*27 bytes
    - payload: N*783 bytes

(A)

(B)

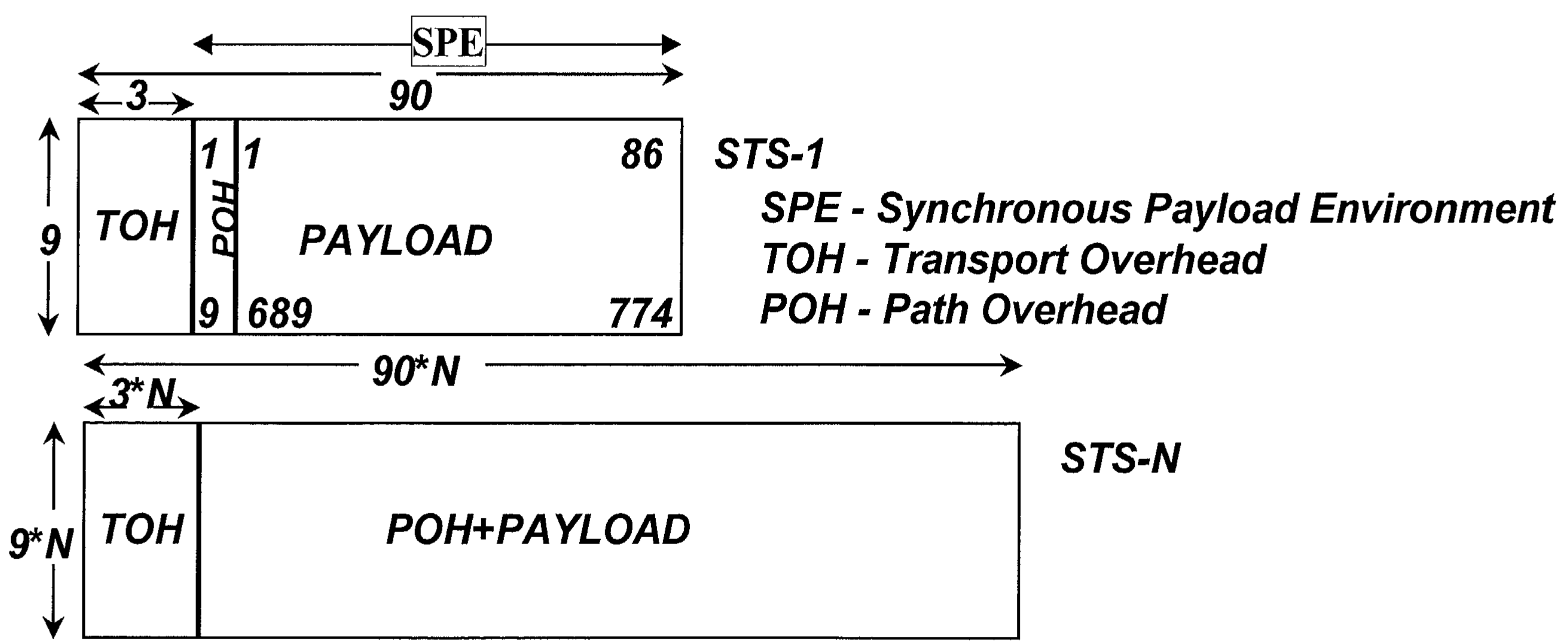
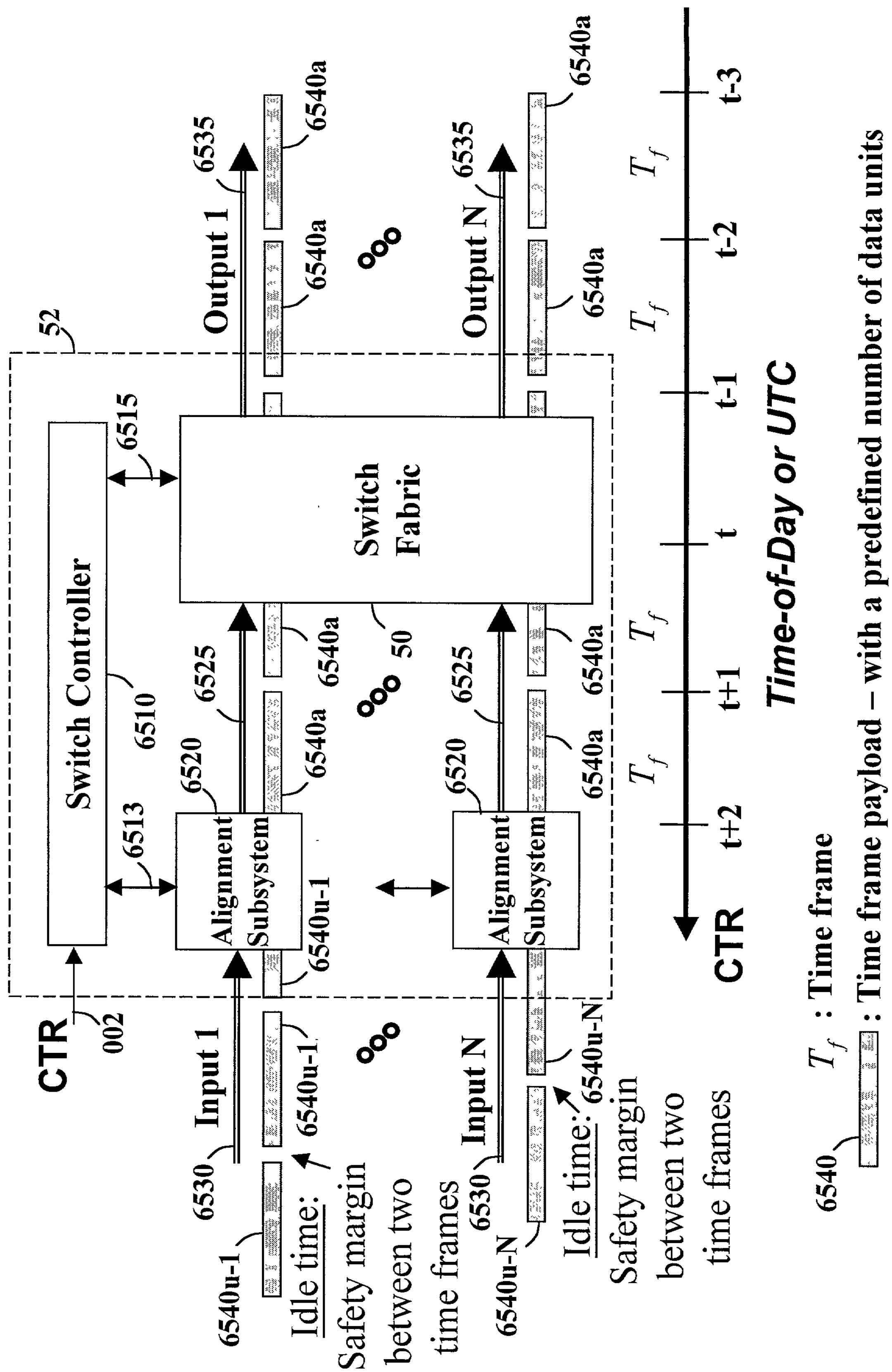


FIG. 65


CTR
002
52
Switch Controller
6510
6513
6515
Alignment Subsystem
Alignment Subsystem
6520
Switch Fabric
50
Input 1
Input N
6530
6525
Output 1
Output N
6535
6540a
6540u-1
6540u-N
Idle time: Safety margin between two time frames
T_f
t+2
t+1
t
t-1
t-2
t-3
CTR
Time-of-Day or UTC
T_f : Time frame
6540
: Time frame payload – with a predefined number of data units